



Advanced Low Power Schottky Logic – 54ALS51

2-wide 3-Input, 2-wide 2-Input AND-OR-Invert Gate IC in bare die form

Rev 1.1
24/01/24

Description

The 54ALS51 is fabricated using a 2µm 40V Bipolar process. The device consists of two independent combinations of gates each performing the logic AND-OR-INVERT function. The IC integrates one 2-wide 3-input gates and one 2-wide 2-input gates each performing Boolean functions $1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$ and $2Y = (2A \cdot 2B) + (2C \cdot 2D)$ respectively. All inputs are protected against ESD and excess voltage transients.

Features:

- High speed – 14ns (Max) propagation delay
- Full Military Temperature Range
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

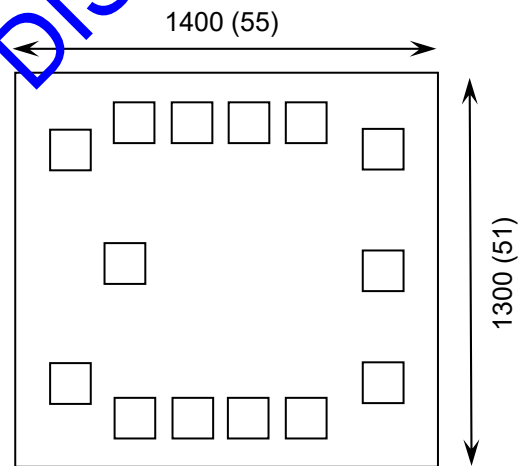
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- ~~***~~ Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

| | | |
|------------------------|----------------------------|------------|
| Die Size (Unsawn) | 1400 x1300 55 x 51 | µm mils |
| Minimum Bond Pad Size | 130 x 130 5.12 x 5.12 | µm mils |
| Die Thickness | 350 (±20) 13.78 (±0.79) | µm mils |
| Top Metal Composition | Al 1%Si 1.1µm | |
| Back Metal Composition | N/A – Bare Si | |

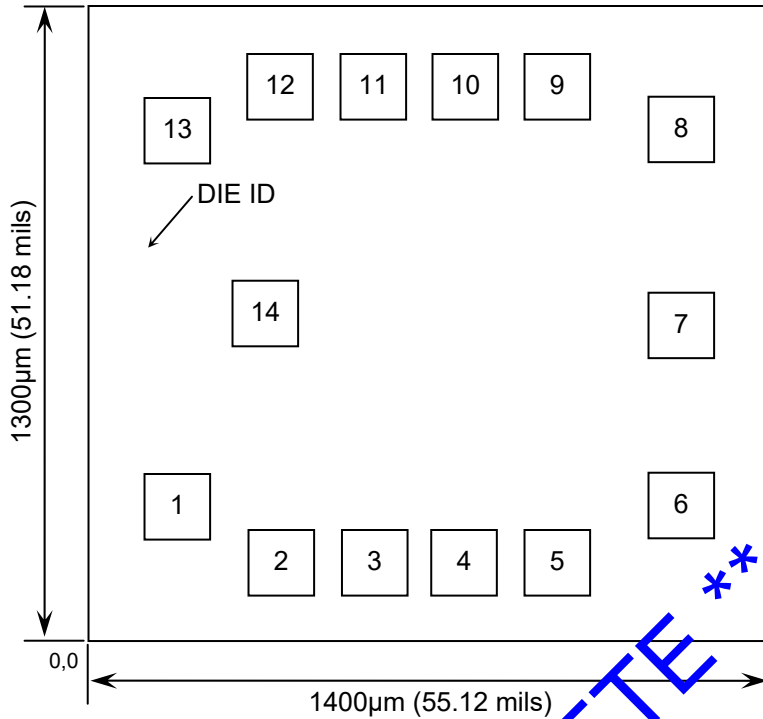




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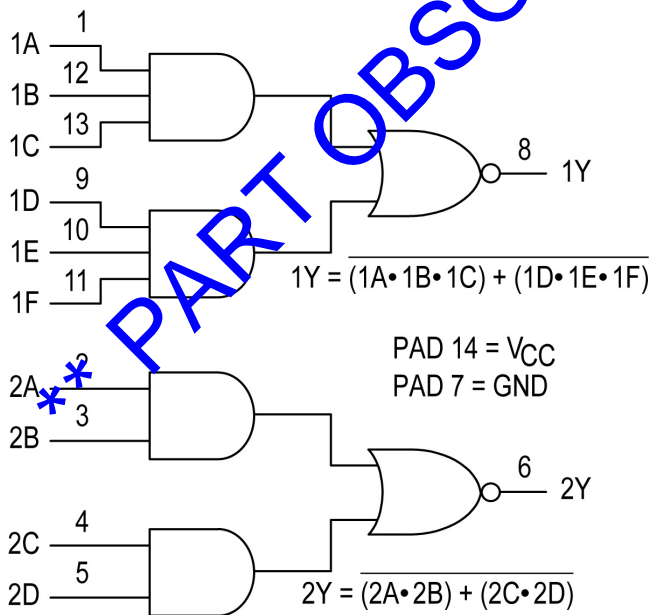
Pad Layout and Functions



| PAD | FUNCTION | COORDINATES (mm) | |
|-----|-----------------|------------------|-------|
| | | X | Y |
| 1 | 1A | 0.110 | 0.215 |
| 2 | 2A | 0.325 | 0.100 |
| 3 | 2B | 0.515 | 0.100 |
| 4 | 2C | 0.705 | 0.100 |
| 5 | 2D | 0.895 | 0.100 |
| 6 | 2Y | 1.150 | 0.215 |
| 7 | GND | 1.150 | 0.585 |
| 8 | 1Y | 1.150 | 0.985 |
| 9 | 1D | 0.895 | 1.070 |
| 10 | 1E | 0.705 | 1.070 |
| 11 | 1F | 0.515 | 1.070 |
| 12 | 1B | 0.325 | 1.070 |
| 13 | 1C | 0.110 | 0.985 |
| 14 | V _{CC} | 0.295 | 0.610 |

CONNECT CHIP BACK TO GND

Logic Diagram



Truth Table

| INPUTS | | | | | | OUTPUT |
|------------------------|----|----|----|--------|----|--------|
| 1A | 1B | 1C | 1D | 1E | 1F | 1Y |
| H | H | H | X | X | X | L |
| X | X | X | H | H | H | L |
| All other combinations | | | | | | H |
| INPUTS | | | | OUTPUT | | |
| 2A | 2B | 2C | 2D | 2Y | | |
| H | H | X | X | L | | |
| X | X | H | H | L | | |
| All other combinations | | | | H | | |

H = High level (steady state)
L = Low level (steady state)
X = don't care





Absolute Maximum Ratings¹

| PARAMETER | SYMBOL | VALUE | UNIT |
|---------------------------|-----------|------------|------|
| DC Supply Voltage | V_{CC} | 7.0 | V |
| DC Input Voltage | V_{IN} | 7.0 | V |
| Storage Temperature Range | T_{STG} | -65 to 150 | °C |

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|-----------------------------|----------|-----|------|-------|
| Supply Voltage | V_{CC} | 4.5 | 5.5 | V |
| High-Level Input Voltage | V_{IH} | 2 | - | V |
| Low-Level Input Voltage | V_{IL} | - | 0.7 | V |
| High-Level Output Current | I_{OH} | - | -0.4 | mA |
| Low-Level Output Current | I_{OL} | - | 4 | mA |
| Operating Temperature Range | T_J | -55 | +125 | °C |

DC Electrical Characteristics² $T_J = -55^{\circ}\text{C}$ to 125°C unless otherwise specified

| PARAMETER | SYMBOL | CONDITIONS | LIMITS | | | UNITS |
|------------------------------------|----------|--|------------|------|------|---------------|
| | | | MIN | TYP | MAX | |
| Minimum High-Level Input Voltage | V_{IH} | - | 2 | - | - | V |
| Maximum Low-Level Input Voltage | V_{IL} | - | - | - | 0.7 | V |
| Input Clamp Diode Voltage | V_{IK} | $V_{CC} = \text{MIN}$ $I_{IN} = -18\text{mA}$ | - | - | -1.5 | V |
| Output Voltage High | V_{OH} | $V_{CC} = \text{MIN}, I_{OH} = \text{MAX}$ $V_{IN} = V_{IL}$ or V_{IH} per Truth Table | $V_{CC}-2$ | - | - | V |
| Output Voltage Low | V_{OL} | $V_{CC} = V_{CC} \text{ MIN}$ $I_{OH} = \text{MAX}$ $V_{IN} = V_{IL}$ or V_{IH} per Truth Table | - | 0.25 | 0.4 | V |
| Input Current | I_{IN} | $V_{CC} = \text{MAX}, V_{IN} = 7.0\text{V}$ | - | - | 0.1 | mA |
| Input High Current | I_{IH} | $V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$ | - | - | 20 | μA |
| Input Low Current | I_{IL} | $V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$ | - | - | -0.1 | mA |
| Short Circuit Current ³ | I_{OS} | $V_{CC} = \text{MAX}$ | -20 | - | -112 | mA |
| Power Supply Current (Total) | I_{CC} | $V_{CC} = \text{MAX}$, Output High | - | - | 1.2 | mA |
| | | $V_{CC} = \text{MAX}$, Output Low | - | - | 1.5 | |

2. All typical values @ $V_{CC} = 5\text{V}$, $T_J = 25^{\circ}\text{C}$. 3. Not more than one output should be shorted at a time, nor for more than 1 second.



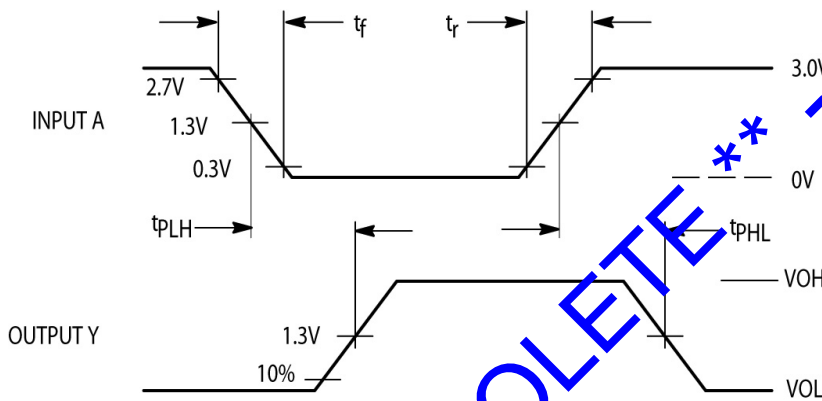


AC Electrical Characteristics⁴

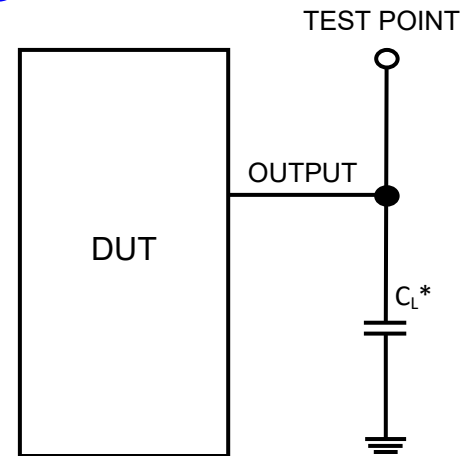
| PARAMETER | SYMBOL | CONDITIONS | LIMITS | | | UNITS |
|---------------------------------|-----------|--|--------|-----|-----|-------|
| | | | MIN | TYP | MAX | |
| Turn-Off Delay, Input to Output | t_{PLH} | $V_{CC} = 5V, C_L = 50pF, R_L = 500\Omega$ | 2 | - | 14 | ns |
| Turn-On Delay, Input to Output | t_{PHL} | $V_{CC} = 5V, C_L = 50pF, R_L = 500\Omega$ | 3 | - | 12 | |

4. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform



Test Circuit



* Includes all probe and jig capacitance

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