Advanced Low Power Schottky Logic - 54ALS174

Hex D-type Flip-Flop in bare die form

Rev 1.1
20/01/24

Description

The 54ALS174 Hex D-type Flip-Flop is fabricated using a 2µm 40V Bipolar process. The device is comprised of six flip-flops each having independent data input and data output. Load and clear is simultaneous, triggered by common clock and master reset respectively. D-Input levels transfer to Q output with the positive clock pulse.

Features:

- High speed – 2ns (Min) propagation delay
- Full Military Temperature Range
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

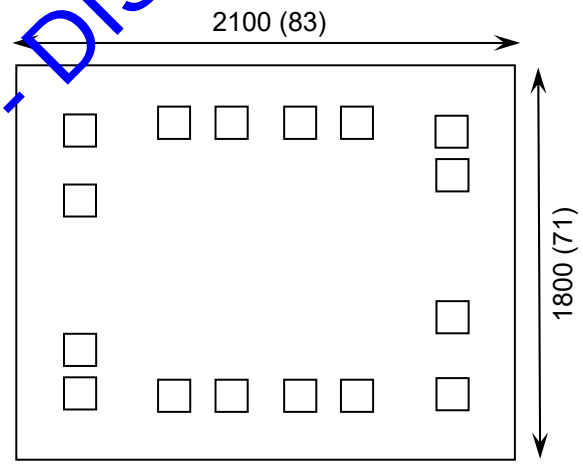
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	2100 x 1800 83 x 71	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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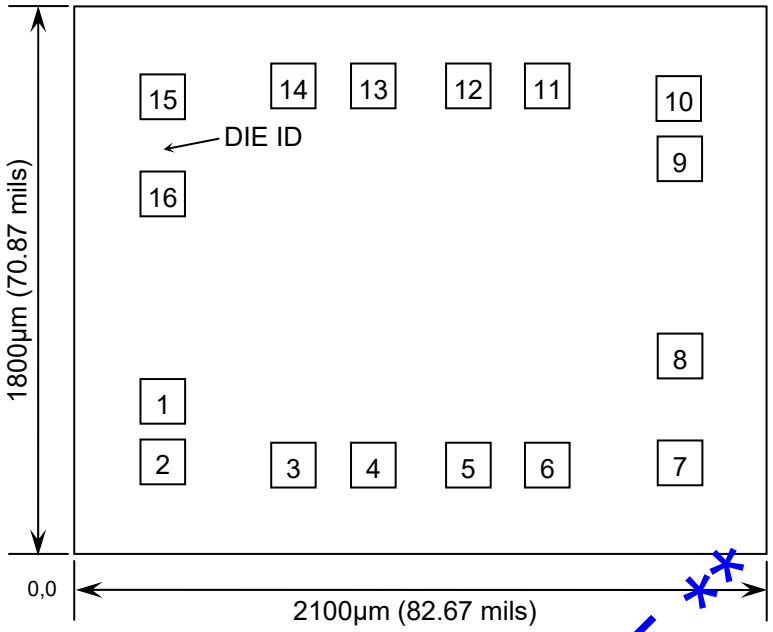
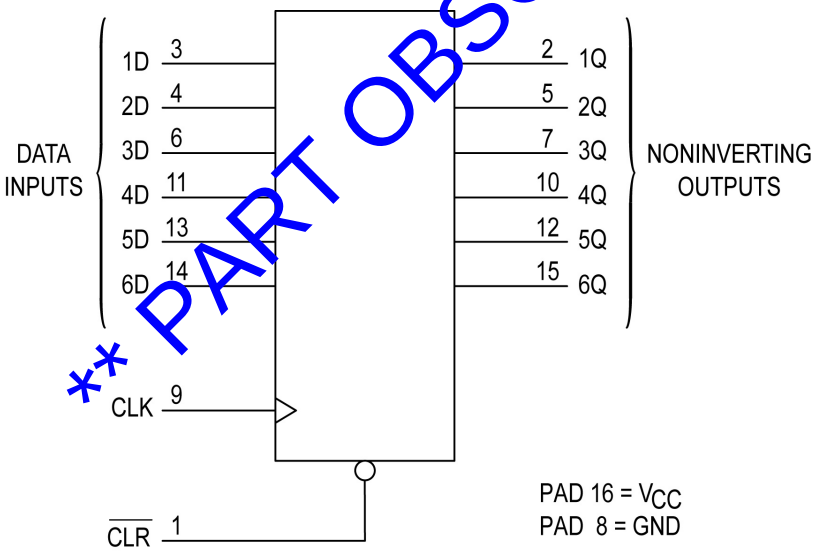
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{CLR}$	0.200	0.435
2	1Q	0.200	0.240
3	1D	0.600	0.200
4	2D	0.840	0.200
5	2Q	1.130	0.200
6	3D	1.370	0.200
7	3Q	1.770	0.240
8	GND	1.770	0.590
9	CLK	1.770	1.240
10	4Q	1.770	1.435
11	4D	1.370	1.470
12	5Q	1.130	1.470
13	5D	0.840	1.470
14	6D	0.600	1.470
15	6Q	0.200	1.435
16	V_{CC}	0.200	1.120
CONNECT CHIP BACK TO GND			

Logic Diagram



Function Table

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Q0

H = High level (steady state)
L = Low level (steady state)
⎍ = Low-to-High clock transition
X = Don't care

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{CC}	7.0	V
DC Input Voltage	V_{IN}	7.0	V
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
High-Level Input Voltage	V_{IH}	2	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
High-Level Output Current	I_{OH}	-	-0.4	mA
Low-Level Output Current	I_{OL}	-	4	mA
Operating Temperature Range	T_J	-55	+125	°C

DC Electrical Characteristics[2] T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum High-Level Input Voltage	V_{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-	-	-	0.8	V
Input Clamp Diode Voltage	V_{IK}	V_{CC} = MIN, I_{IN} = -18mA	-	-	-1.5	V
Output Voltage High	V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = -0.4mA	V_{CC} -2	-	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V, I_{OL} = 4mA	-	0.25	0.4	V
Input Current	I_{IN}	V_{CC} = 5.5V, V_{IN} = 7V	-	-	0.1	mA
Input High Current	I_{IH}	V_{CC} = 5.5V, V_{IN} = 2.7V	-	-	20	µA
Input Low Current	I_{IL}	V_{CC} = 5.5, V_{IN} = 0.4V	-	-	-0.1	mA
Output Current[3]	I_O	V_{CC} = 5.5, V_{OUT} = 2.25V	-20	-	-112	mA
Power Supply Current (Total)	I_{CC}	V_{CC} = 5.5V , V_{IN} = 4.5V	-	11	19	mA

2. All typical values @ V_{CC} = 5V, T_J = 25°C.

3. Output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}

AC Electrical Characteristics[4] T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Maximum Clock Frequency	f_{max}	5V ±10%	C_L = 50pF, R_L = 500Ω	40	-	-	MHz
Maximum Propagation Delay, $\overline{CLR}$ to Q (Figure 1)	t_{PLH},	5V ±10%	C_L = 50pF, R_L = 500Ω	3	-	20	ns
	t_{PHL}			5	-	30	
Maximum Propagation Delay, CLK to Q (Figure 1)	t_{PLH},	5V ±10%	C_L = 50pF, R_L = 500Ω	3	-	20	ns
	t_{PHL}			5	-	24	

Timing Requirements[4] T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Minimum Pulse Width, CLK (Figure 3)	$t_{w(H)}$, $t_{w(L)}$,	5V ±10%	C_L = 50pF, R_L = 500Ω	12.5	-	-	ns
Minimum Pulse Width, $\overline{CLR}$ (Figure 3)	$t_{w(L)}$	5V ±10%	C_L = 50pF, R_L = 500Ω	15	-	-	ns
Minimum Setup Time Before CLK (Figure 2)	t_{SU}	5V ±10%	Data, C_L = 50pF, R_L = 500Ω	15	-	-	ns
Minimum Setup Time Before CLK (Figure 2)	t_{SU}	5V ±10%	$\overline{CLR}$ Inactive, C_L = 50pF, R_L = 500Ω	8	-	-	ns
Hold Time, Data after CLK (Figure 2)	t_h	5V ±10%	C_L = 50pF, R_L = 500Ω s	0	-	-	ns

4. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform

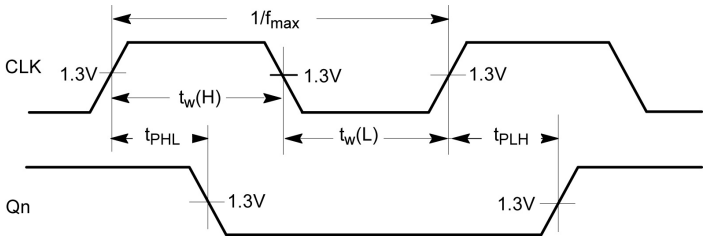


Figure 1 – Propagation Delay
Clock to Output and minimum Clock Frequency

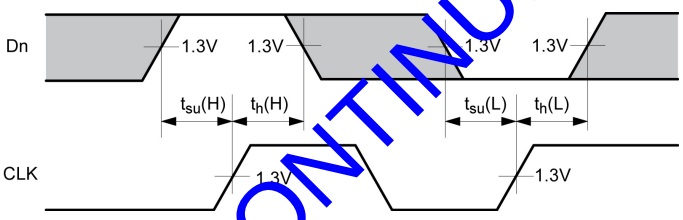


Figure 2 – Data Setup and Hold Times

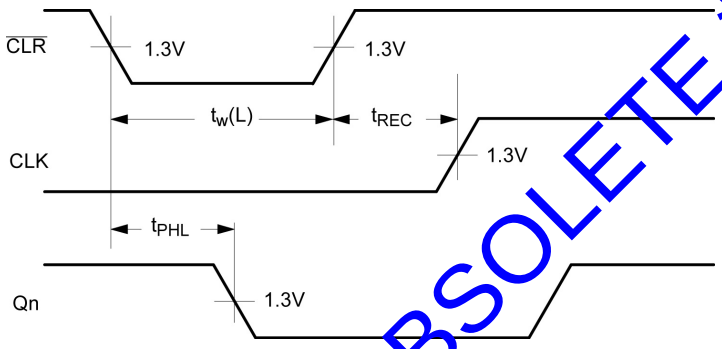
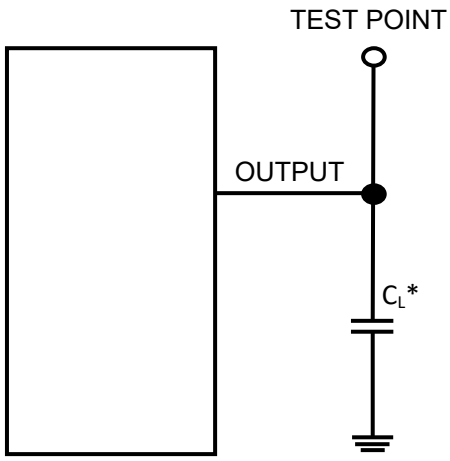


Figure 3 – Reset to Output, Reset to Clock Recovery

Test Circuit



* Includes all probe and jig capacitance