Advanced Low Power Schottky Logic – 54ALS00

Quad 2-Input NAND Gates in bare die form

Rev 1.1
23/01/24

Description

54ALS00 provides x4 independent 2-input NAND gates performing the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$. The device is fabricated using a 1.5µm 40V Bipolar process. Internal circuitry comprises of 3 stages and includes buffered outputs for high noise immunity and stability. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

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Features:

- High speed – 3ns (Min) propagation delay
- Full Military Temperature Range
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

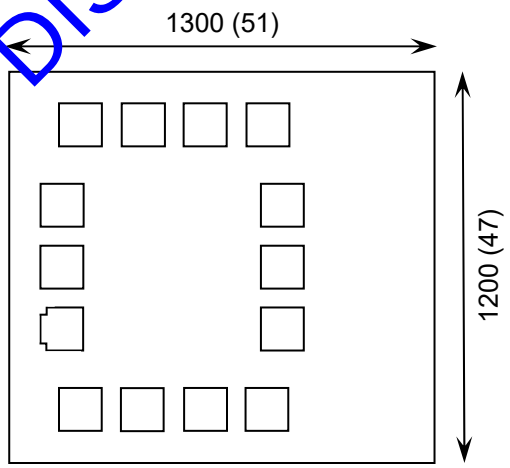
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (300 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1300 x 1200 51 x 47	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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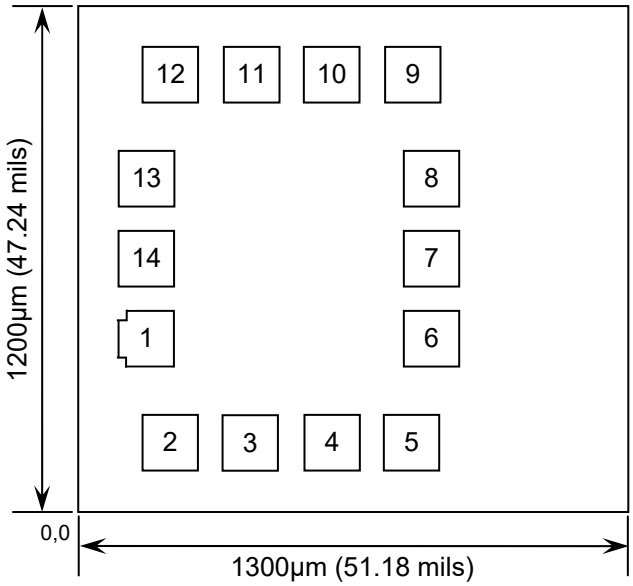
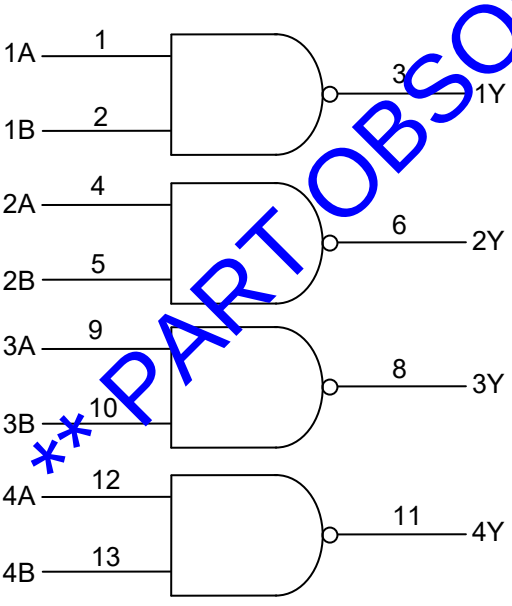
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.100	0.345
2	1B	0.155	0.100
3	1Y	0.345	0.100
4	2A	0.535	0.100
5	2B	0.725	0.100
6	2Y	0.770	0.345
7	GND	0.770	0.535
8	3Y	0.770	0.725
9	3A	0.725	0.970
10	3B	0.535	0.970
11	4Y	0.345	0.970
12	4A	0.155	0.970
13	4B	0.100	0.725
14	V_{CC}	0.100	0.535
CONNECT CHIP BACK TO GND			

Logic Diagram



Function Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L
H = High level (steady state) L = Low level (steady state)		

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{CC}	7.0	V
DC Input Voltage	V_{IN}	7.0	V
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
High-Level Input Voltage	V_{IH}	2	-	V
Low-Level Input Voltage	V_{IL}	-	0.7	V
High-Level Output Current	I_{OH}	-	-0.4	mA
Low-Level Output Current	I_{OL}	-	4	mA
Operating Temperature Range	T_J	-55	+125	°C

DC Electrical Characteristics[2] T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum High-Level Input Voltage	V_{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-	-	-	0.7	V
Input Clamp Diode Voltage	V_I	V_{CC} = MIN, I_{IN} = -18mA	-	-	-1.5	V
Output Voltage High	V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = -0.4mA	V_{CC} -2	-	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V, I_{OL} = 4mA	-	0.25	0.4	V
Input Current	I_{IN}	V_{CC} = 5.5V, V_{IN} = 7V	-	-	0.1	mA
Input High Current	I_{IH}	V_{CC} = 5.5V, V_{IN} = 2.7V	-	-	20	µA
Input Low Current	I_{IL}	V_{CC} = 5.5, V_{IN} = 0.4V	-	-	-0.1	mA
Output Current[3]	I_O	V_{CC} = 5.5, V_{OUT} = 2.25V	-20	-	-112	mA
Power Supply Current (Total)	I_{CCH}	V_{CC} = 5.5V , V_{IN} = 4.5V	-	0.5	0.85	mA
	I_{CCL}	V_{CC} = 5.5V , V_{IN} = 0V	-	1.5	3	

2. All typical values @ V_{CC} = 5V, T_J = 25°C.

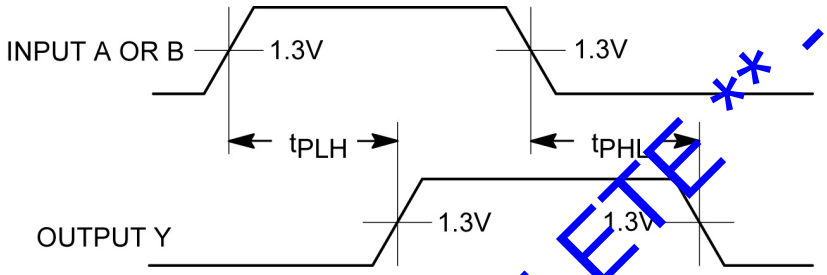
3. Output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}

AC Electrical Characteristics[4] T_J = -55°C to 125°C unless otherwise specified

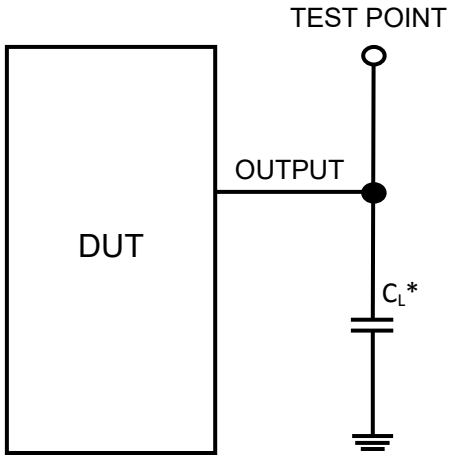
PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay, A or B to output Y	t_{PLH}	V_{CC} = 4.5 to 5.5V, C_L = 50pF, R_L = 500Ω	3	-	15	ns
	t_{PHL}		2	-	9	

4. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform



Test Circuit



* Includes all probe and jig capacitance