Advanced CMOS TTL Input – 54ACT74

Dual D-Type Flip-Flop Logic IC with Set and Reset in bare die form

Rev 1.0
21/11/19

Description

The 54ACT74 is fabricated using a 1.5µm advanced 5V CMOS process & consists of two identical, independent data type flip-flops. Each flip-flop has separate data, set, reset, clock inputs & Q,$\overline{Q}$ outputs. The device can be used in Shift Register applications and also Counter or Toggle applications by connecting Q output to the data input. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is clock independent and accomplished by a high level on the respective Set or Reset line.

Features:

- Inputs directly accept TTL
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Outputs Source/Sink 24 mA
- Asynchronous Set-Reset Capability
- Lower power alternative to bipolar logic
- Functionally compatible with bipolar 54LS74
- Direct drop in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

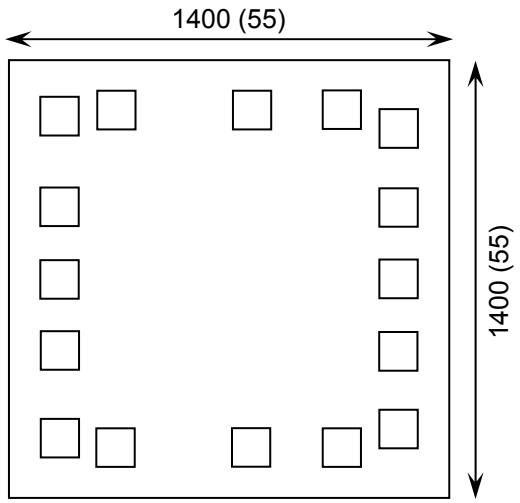
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



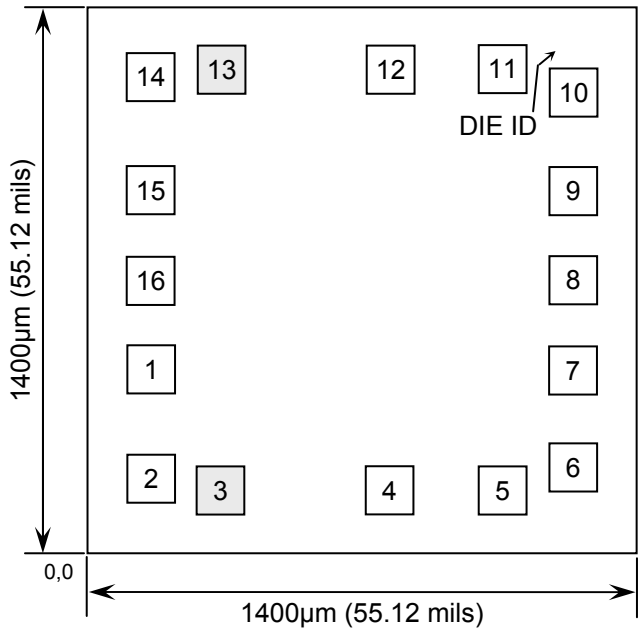
Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

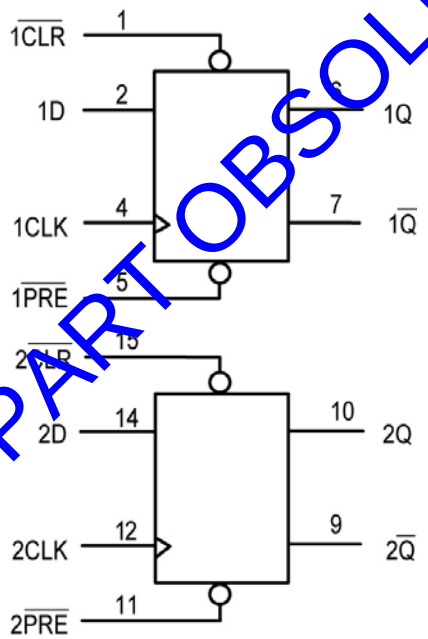
Die Size (Unsawn)	1400 x 1400 55 x 55	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$1\overline{CLR}$	0.100	0.410
2	1D	0.100	0.130
3	NO CONNECT	0.280	0.100
4	1CLK	0.710	0.100
5	$1\overline{PRE}$	1.00	0.100
6	1Q	1.180	0.160
7	$1\overline{Q}$	1.180	0.410
8	GND	1.180	0.640
9	$2\overline{Q}$	1.180	0.870
10	2Q	1.180	1.120
11	$2\overline{PRE}$	1.00	1.180
12	2CLK	0.710	1.180
13	NO CONNECT	0.280	1.180
14	2D	0.100	1.160
15	$2\overline{CLR}$	0.100	0.870
16	V_{CC}	0.100	0.640
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



PAD 16 = V_{CC}
PAD 8= GND

Truth Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

* BOTH OUTPUTS WILL REMAIN HIGH AS LONG AS SET AND RESET ARE LOW, OUTPUT STATES ARE UNPRE-DICTABLE IF SET AND RESET GO HIGH SIMULTANEOUSLY.

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input or Output Voltage (Referenced to GND)	V_{IN}, V_{OUT}	-0.5 to V_{CC}+0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}	±20	mA
Output Current (per Pad)	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages Referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Output current - High		I_{OH}	-	-24	mA
Output current - Low		I_{OL}	-	24	mA
Input Rise or Fall rate (V_{IN} from 0.8V to 2V)	V_{CC} = 4.5V	$\Delta t/\Delta V$	0	10	ns/V
	V_{CC} = 5.5V		0	8	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS 25°C	LIMITS 85°C	LIMITS FULL RANGE[4]	UNITS
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum Low-Level Output Voltage	V_{OL}	4.5V	I_{OUT} = 50µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OL} = 24mA	0.36	0.44	0.50	V
		5.5V		0.36	0.44	0.50	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5,6] I_{OL} = 50mA	-	-	1.65	V
		5.5V		-	-	1.65	

4. -55˚C ≤ T_J ≤ +125˚C **5.** All outputs loaded; thresholds on input associated with output under test. **6.** Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	4.5V	I_{OUT} = -50µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OL} = -24mA	3.86	3.76	3.70	V
		5.5V		4.86	4.76	4.70	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5,6] I_{OL} = -50mA	-	-	3.86	V
		5.5V		-	-	3.86	
Maximum Input Leakage Current	I_{IN}	5.5V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Additional Maximum I_{CC} / Input	ΔI_{CCT}	5.5V	V_{IN} = V_{CC} -2.1V	0.6	1.5	1.6	mA
Minimum Dynamic Output Current[7]	I_{OLD}	5.5V	V_{OLD} = 1.65V Max	-	75	50	mA
	I_{OHD}	5.5V	V_{OHD} = 3.86V Min	-	-75	-50	
Maximum Quiescent Supply Leakage Current	I_{CC}	5.5V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	4	40	80	µA

7. Maximum test duration 2ms, one output loaded at a time.

AC Electrical Characteristics[8]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency	f_{max}	5V ±10%	-	145	125	85	MHz
Maximum Propagation Delay, $\overline{CLK}$ to Q or $\overline{Q}$ (Figure1)	t_{PLH},	5V ±10%	C_L = 50pF, Input t_r = t_f = 3ns	11	13	14	ns
	t_{PHL}			10	11.5	12	
Maximum Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$ (Figure 2)	t_{PLH},	5V ±10%	C_L = 50pF, Input t_r = t_f = 3ns	9.5	10.5	11.5	ns
	t_{PHL}			10	11.5	12.5	
Maximum Input Capacitance	C_{IN}	5V ±10%	V_{IN} = V_{CC} or GND	4.5	4.5	4.5	pF
Power Dissipation Capacitance[9]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	TYPICAL			pF
				35			

8. Not production tested in die form, characterized by chip design and tested in package.
9. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[8]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE*	
Minimum Setup Time, D to CLK (Figure 3)	t_{SU}	5V ±10%	C_L = 50pF, Input t_r = t_f = 3ns	3	3.5	4	ns
Minimum Hold Time, CLK to D (Figure 3)	t_h	5V ±10%	C_L = 50pF, Input t_r = t_f = 3ns	1	1	1	ns
Minimum Pulse Width, CLK, $\overline{PRE}$, $\overline{CLR}$ (Figure 1)	t_w	5V ±10%	C_L = 50pF, Input t_r = t_f = 3ns	5	6	7	ns
Maximum Recovery Time, $\overline{PRE}$ or CLR to CLK (Figure 2)	t_{rec}	5V ±10%	C_L = 50pF, Input t_r = t_f = 3ns	0	0	0	ns

Switching Waveforms

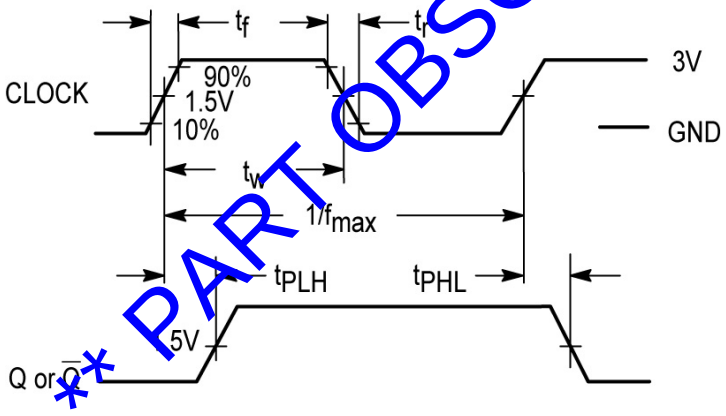


Figure 1 – Data, Clock and Output

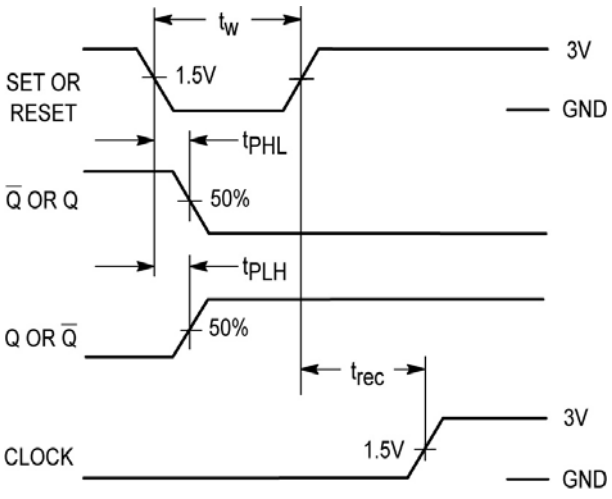


Figure 2 – Set, Reset, Clock and Output

Switching Waveforms continued

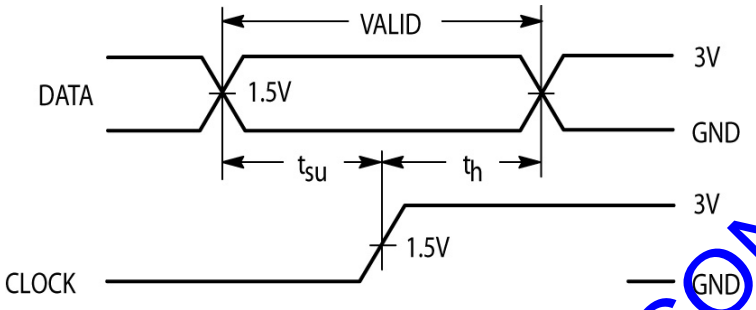
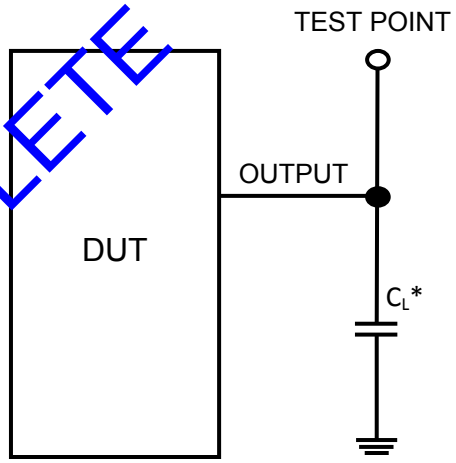


Figure 3 – Clock to Data

Test Circuit



* Includes all probe and jig capacitance