



Advanced CMOS TTL Input – 54ACT38

Quad 2-input NAND buffer (open drain) in bare die form

Rev 1.0
18/01/21

Description

54ACT38 provides x4 independent 2-input NAND gates performing the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$. The device is fabricated using an advanced 1.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power consumption. The provision of open-drain outputs enables implementation of active-low wired-OR or active-high wired-AND functionality. Device inputs directly accept both standard CMOS and LSTTL outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Open-drain output for wired-OR/wired-AND function
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 54LS38, 54F38
- Lower power alternative to bipolar logic
- Full military temperature range.

Ordering Information

The following part suffixes apply:

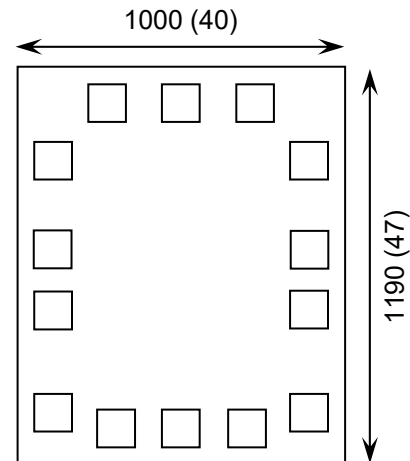
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For more information on LAT flows please see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- *** Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

| | | |
|------------------------|----------------------------|------------|
| Die Size (Unsawn) | 1000 x 1190 40 x 47 | µm mils |
| Minimum Bond Pad Size | 100 x 100 4 x 4 | µm mils |
| Die Thickness | 350 (±20) 13.78 (±0.79) | µm mils |
| Top Metal Composition | Al 1%Si 1.1µm | |
| Back Metal Composition | N/A – Bare Si | |

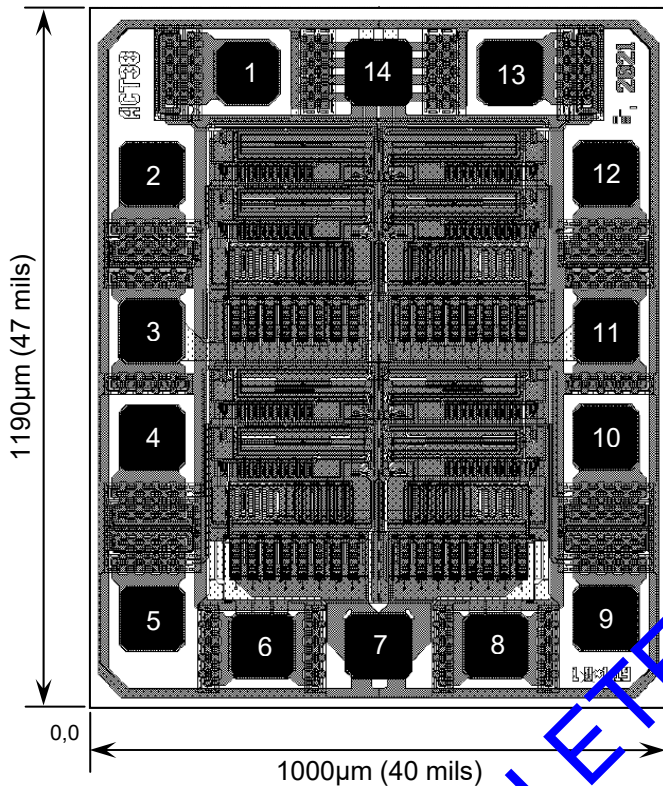




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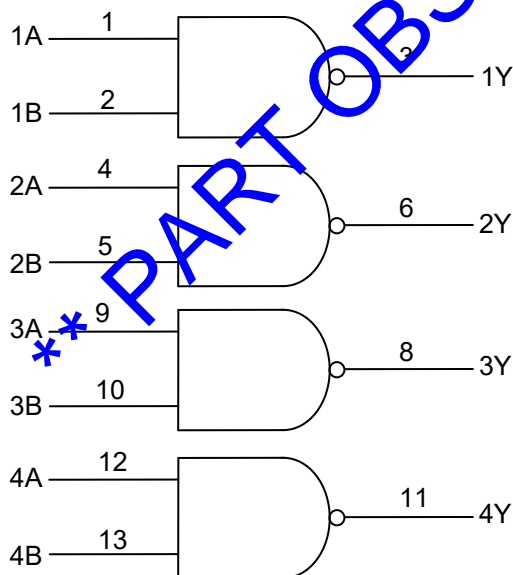
Pad Layout and Functions



| PAD | FUNCTION | COORDINATES (mm) | |
|-----|-----------------|------------------|-------|
| | | X | Y |
| 1 | 1A | 0.250 | 0.980 |
| 2 | 1B | 0.100 | 0.820 |
| 3 | 1Y | 0.100 | 0.580 |
| 4 | 2A | 0.100 | 0.420 |
| 5 | 2B | 0.100 | 0.140 |
| 6 | 2Y | 0.270 | 0.100 |
| 7 | GND | 0.450 | 0.100 |
| 8 | 3Y | 0.670 | 0.100 |
| 9 | 3A | 0.790 | 0.140 |
| 10 | 3B | 0.790 | 0.420 |
| 11 | 4Y | 0.790 | 0.590 |
| 12 | 4A | 0.790 | 0.820 |
| 13 | 4B | 0.650 | 0.980 |
| 14 | V _{CC} | 0.450 | 0.980 |

CONNECT CHIP BACK TO V_{CC} OR FLOAT

Logic Diagram



Truth Table

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | Z |
| L | H | Z |
| H | L | Z |
| H | H | L |

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance state





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Absolute Maximum Ratings¹

| PARAMETER | SYMBOL | VALUE | UNIT |
|--|-------------------|----------------------|------|
| DC Supply Voltage (Referenced to GND) | V_{CC} | -0.5 to +7.0 | V |
| DC Input or Output Voltage (Referenced to GND) | V_{IN}, V_{OUT} | -0.5 to $V_{CC}+0.5$ | V |
| Storage Temperature Range | T_{STG} | -65 to 150 | °C |
| Input Current (per Pad) | I_{IN} | ±20 | mA |
| Output Current (per Pad) | I_{OUT} | ±50 | mA |
| DC Supply Current, V_{CC} or GND, per pad | I_{CC} | ±50 | mA |
| Power Dissipation in Still Air ² | P_D | 500 | mW |

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic SSOP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages Referenced to GND)

| PARAMETER | SYMBOL | MIN | MAX | UNITS | |
|--|---------------------|-----------------|----------|-------|------|
| DC Supply Voltage | V_{CC} | 4.5 | 5.5 | V | |
| DC Input or Output Voltage | V_{IN}, V_{OUT} | 0 | V_{CC} | V | |
| Operating Temperature Range | T_J | -55 | +125 | °C | |
| Output current - High | I_{OH} | - | -24 | mA | |
| Output current - Low | I_{OL} | - | 24 | mA | |
| Input Rise or Fall rate (V_{IN} from 0.8V to 2V) | $\Delta t/\Delta V$ | $V_{CC} = 4.5V$ | 0 | 10 | ns/V |
| | | $V_{CC} = 5.5V$ | 0 | 8 | |

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

| PARAMETER | SYMBOL | V_{CC} | CONDITIONS | LIMITS | | | UNITS |
|----------------------------------|----------|----------|--|--------|------|-------------------------|-------|
| | | | | 25°C | 85°C | FULL RANGE ⁴ | |
| Minimum High-Level Input Voltage | V_{IH} | 4.5V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | 2 | 2 | 2 | V |
| | | 5.5V | | 2 | 2 | 2 | |
| Maximum Low-Level Input Voltage | V_{IL} | 4.5V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | 0.8 | 0.8 | 0.8 | V |
| | | 5.5V | | 0.8 | 0.8 | 0.8 | |
| Minimum Low-Level Output Voltage | V_{OL} | 4.5V | $I_{OUT} = 50\mu A$ | 0.1 | 0.1 | 0.1 | V |
| | | 5.5V | | 0.1 | 0.1 | 0.1 | |
| | | 4.5V | $V_{IN} = V_{IL}$ or V_{IH} ⁵ | 0.36 | 0.44 | 0.50 | V |
| | | 5.5V | $I_{OL} = 24mA$ | 0.36 | 0.44 | 0.50 | |
| | | 4.5V | $V_{IN} = V_{IL}$ or V_{IH} ^{5,6} | - | - | 1.65 | V |
| | | 5.5V | $I_{OL} = 50mA$ | - | - | 1.65 | |

4. -55°C ≤ T_J ≤ +125°C 5. All outputs loaded; thresholds on input associated with output under test. 6. Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C





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DC Electrical Characteristics Continued (Voltages referenced to GND)

| PARAMETER | SYMBOL | V _{CC} | CONDITIONS | LIMITS | | | UNITS |
|---|-------------------|-----------------|--|--------|------|-------------------------|-------|
| | | | | 25°C | 85°C | FULL RANGE ⁴ | |
| Minimum High-Level Output Voltage | V _{OH} | 4.5V | I _{OUT} = -50μA | 4.4 | 4.4 | 4.4 | V |
| | | 5.5V | | 5.4 | 5.4 | 5.4 | |
| | | 4.5V | V _{IN} = V _{IL} or V _{IH} ⁵ | 3.86 | 3.76 | 3.70 | V |
| | | 5.5V | I _{OL} = -24mA | 4.86 | 4.76 | 4.70 | |
| | | 4.5V | V _{IN} = V _{IL} or V _{IH} ^{5,6} | - | - | 3.86 | V |
| | | 5.5V | I _{OL} = -50mA | - | - | 3.86 | |
| Maximum Input Leakage Current | I _{IN} | 5.5V | V _{IN} = V _{CC} or GND | ±0.1 | ±1.0 | ±1.0 | μA |
| Maximum 3-State leakage current | I _{OZ} | 5.5 | V _{OUT} =V _{CC} or GND, V _{IN} = V _{IL} or V _{IH} | ±0.5 | ±2.5 | ±5 | μA |
| Additional Maximum I _{CC} / Input | ΔI _{CCT} | 5.5V | V _{IN} = V _{CC} -2.1V | 0.6 | 1.5 | 1.6 | mA |
| Minimum Dynamic Output Current ⁷ | I _{OLD} | 5.5V | V _{OLD} = 1.65V Max | - | 75 | 50 | mA |
| | I _{OHD} | 5.5V | V _{OHD} = 3.86V Min | - | -75 | -50 | |
| Maximum Quiescent Supply Leakage Current | I _{CC} | 5.5V | V _{IN} = V _{CC} or GND I _{OUT} = 0μA | 4 | 40 | 80 | μA |

7. Maximum test duration 2ms, one output loaded at a time.

AC Electrical Characteristics⁸

| PARAMETER | SYMBOL | V _{CC} | CONDITIONS | LIMITS | | | UNITS |
|---|------------------|-----------------|--|---------|------|-------------------------|-------|
| | | | | 25°C | 85°C | FULL RANGE ⁴ | |
| Maximum Propagation Delay, A or B to Y | t _{PL} | 5V ±10% | GND = 0V, C _L = 50pF, R _L = 500Ω, t _r = t _f = ≤ 2.5ns | 6 | 7 | 13 | ns |
| | t _{PHL} | | | 6 | 7 | 13 | |
| Maximum Propagation Delay, OFF-state to Low | t _{PZL} | 5V ±10% | GND = 0V, C _L = 50pF, R _L = 500Ω, t _r = t _f = ≤ 2.5ns, (Figure1) | 5.1 | 6 | 13 | ns |
| Maximum Propagation Delay, Low to OFF-state | t _{PLZ} | | | 5.0 | 5.3 | 13 | |
| Maximum Input Capacitance | C _{IN} | 5V ±10% | V _{IN} = V _{CC} or GND | 8 | 8 | 8 | pF |
| Power Dissipation Capacitance ⁹ | C _{PD} | - | T _J = 25°C, V _{CC} = 5.0V | TYPICAL | | | pF |
| | | | | 40 | | | |

8. Not production tested in die form, characterized by chip design.

9. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.





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Switching Waveforms

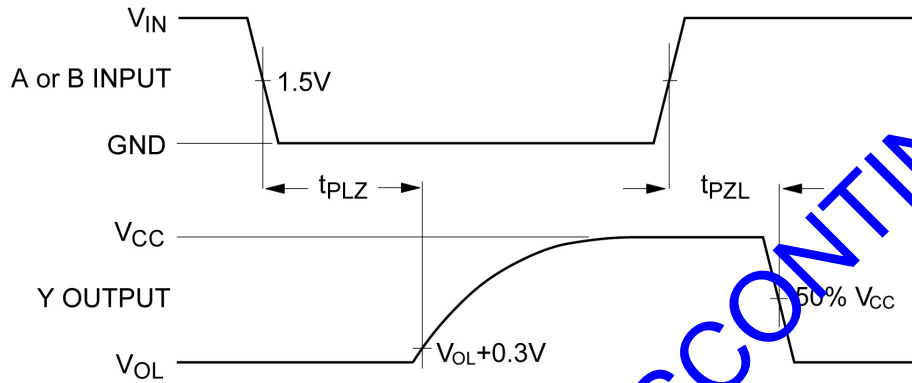
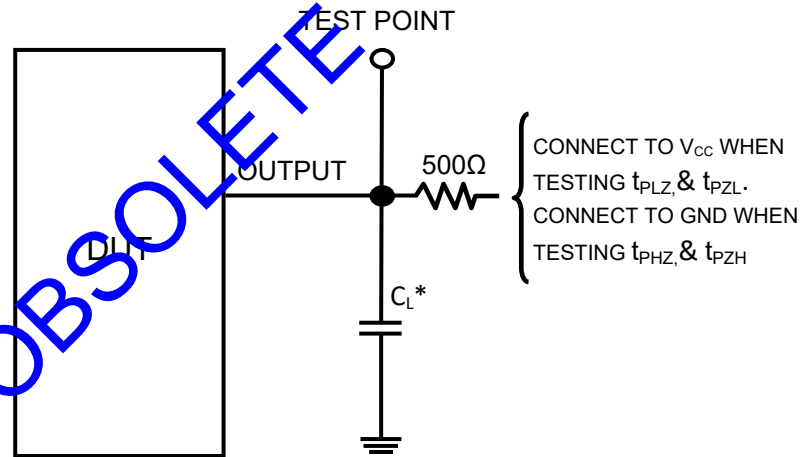


Figure 1 – Propagation Delay, Input A or B to Output Y

Test Circuit



* Includes all probe and jig capacitance

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