Advanced CMOS TTL Input – 54ACT05

Hex Inverter Gate with Open-Drain Outputs in bare die form

Rev 1.0
10/05/19

Description

The 54ACT05 hex inverter gate is fabricated on a 1.5µm advanced 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device contains six independent inverters with open-drain outputs and perform the Boolean function Y = $\bar{A}$. Device outputs can connect with other open-drain outputs to form active LOW wired-OR or active HIGH wired-AND logic functions. Open-drain outputs need pull-up resistors to perform correctly*. Inputs are directly compatible with both standard TTL and CMOS outputs.

Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 54LS05
- Lower power alternative to bipolar logic
- Full Military Temperature Range

Ordering Information

The following part suffixes apply:

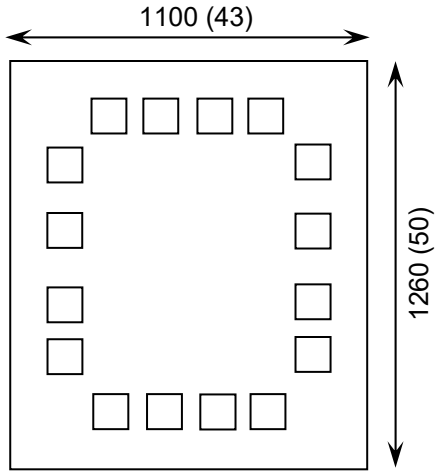
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1100 x 1260 43 x 50	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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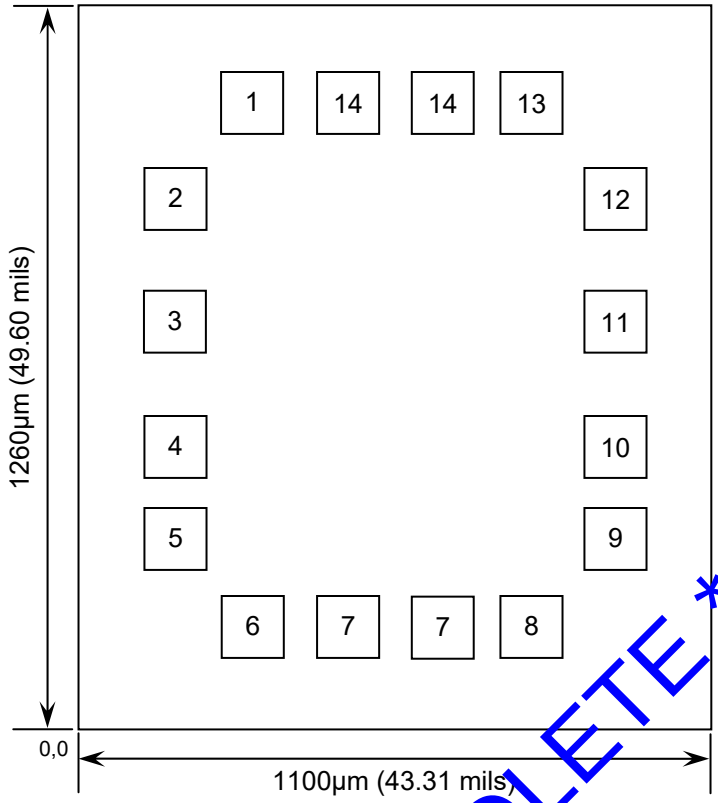
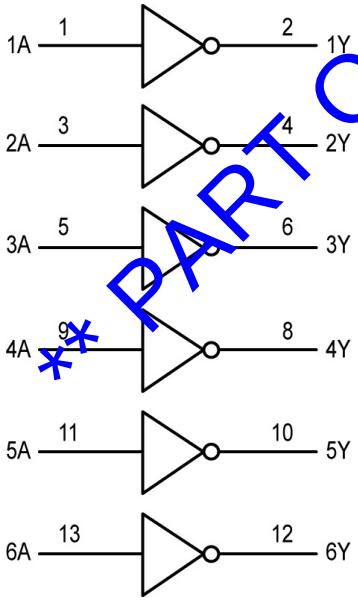
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	1A	260	1035
2	1Y	120	865
3	2A	120	700
4	2Y	120	480
5	3A	120	255
6	3Y	260	115
7	GND	425	115
7	GND	580	115
8	4Y	745	115
9	4A	880	255
10	5Y	880	480
11	5A	880	700
12	6Y	880	865
13	6A	745	1035
14	V_{CC}	580	1035
14	V_{CC}	420	1035
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



$Y = \bar{A}$

Pad 14 = V_{CC}
Pad 7 = GND

Truth Table

INPUTS A	OUTPUT Y
H	L
L	Z

H = High level (steady state)
L = Low level (steady state)
Z = High-impedance off-state

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages Referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Output current - High		I_{OH}	-	-24	mA
Output current - Low		I_{OL}	-	24	mA
Input Rise or Fall rate (V_{IN} from 0.8V to 2V)	V_{CC} = 4.5V	$\Delta t/\Delta V$	0	10	ns/V
	V_{CC} = 5.5V		0	10	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum Low-Level Output Voltage	V_{OL}	4.5V	I_{OUT} = 50µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OL} = 24mA	0.36	0.44	0.50	V
		5.5V		0.36	0.44	0.50	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5,6] I_{OL} = 50mA	-	-	1.65	V
		5.5V		-	-	1.65	

4. -55˚C ≤ T_J ≤ +125˚C **5.** All outputs loaded; thresholds on input associated with output under test. **6.** Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Additional Maximum I_{CC} / Input	ΔI_{CCT}	5.5V	$V_{IN} = V_{CC}$ -2.1V	2.4	2.8	3	mA
Minimum Dynamic Output Current[7]	I_{OLD}	5.5V	V_{OLD} = 1.65V Max	-	75	50	mA
	I_{OHD}	5.5V	V_{OHD} = 3.85V Min	-	-75	-50	
Maximum Quiescent Supply Leakage Current	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0µA	4	40	80	µA

7. Maximum test duration 2ms, one output loaded at a time.

AC Electrical Characteristics[8] V_{CC} = 5.0V ±0.5V

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Output Enable (Figure 1)	t_{PZL}	5.0V	C_L = 50pF	8	8.5	9.3	ns
	t_{PLZ}	5.0V		8.5	9	10.8	
Maximum Input Capacitance	C_{IN}	5.0V	T_J = 25°C	TYPICAL			pF
				4.5			
Power Dissipation Capacitance	C_{PD}	5.0V	T_J = 25°C, C_L = 50pF	30			pF

8. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform

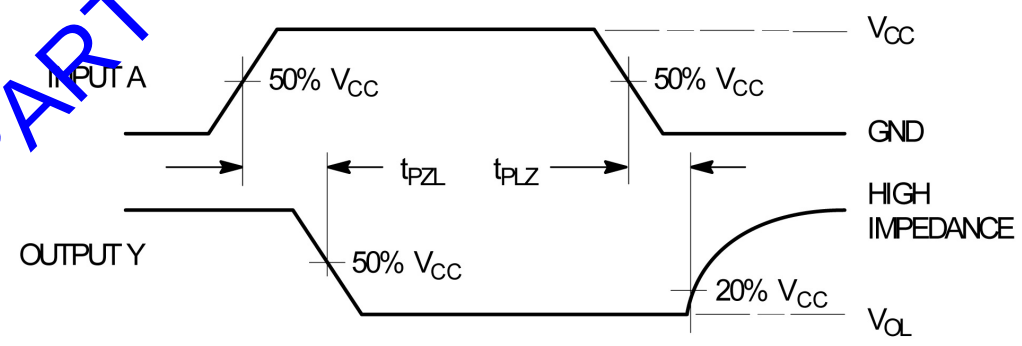
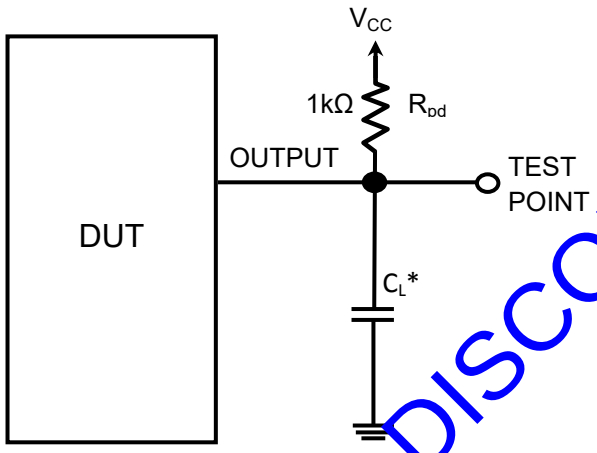


Figure 1 – Propagation Delay

Test Circuit



* Includes all probe and jig capacitance

Figure 2 – Test Circuit