



# Advanced CMOS Logic – 54AC139

## Dual 1-of-4 Decoder / Demultiplexer in bare die form

Rev 1.1  
21/07/20

### Description

The 54AC139 is fabricated using a 1.5µm 5V advanced CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. This device consists of x2 independent 1-of-4 decoders, each decoding a 2 bit address to 1-of-4 active-low outputs. Active-low Selects facilitate the demultiplexing and cascading functions. The demultiplexing function is executed by using the Address inputs to select the desired device output and utilizing the Select as a data input. Inputs accept standard CMOS outputs or LSTTL outputs using pull-up resistors.

### Features:

- Outputs Sink/Source 24mA
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS139
- Full Military Temperature Range.

### Ordering Information

The following part suffixes apply:

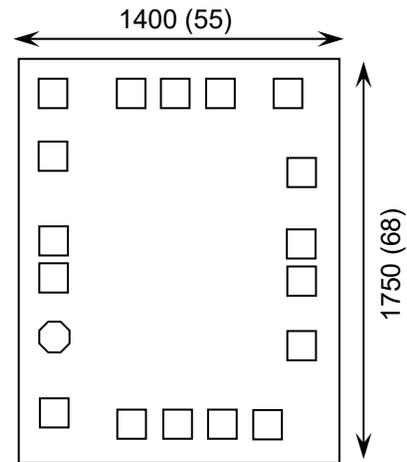
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

### Die Dimensions in µm (mils)



### Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- ~~\*\*\*~~ Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

### Mechanical Specification

Die Size (Unsawn)	1400 x 1750 55 x 68	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

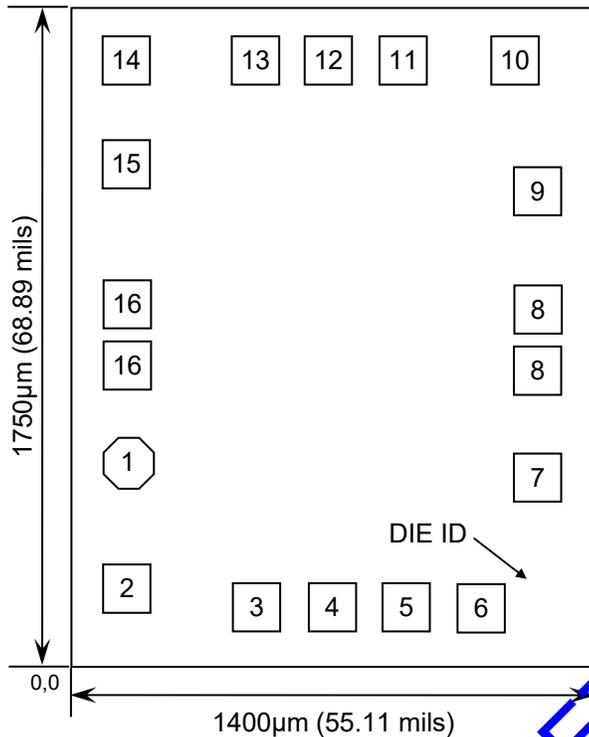




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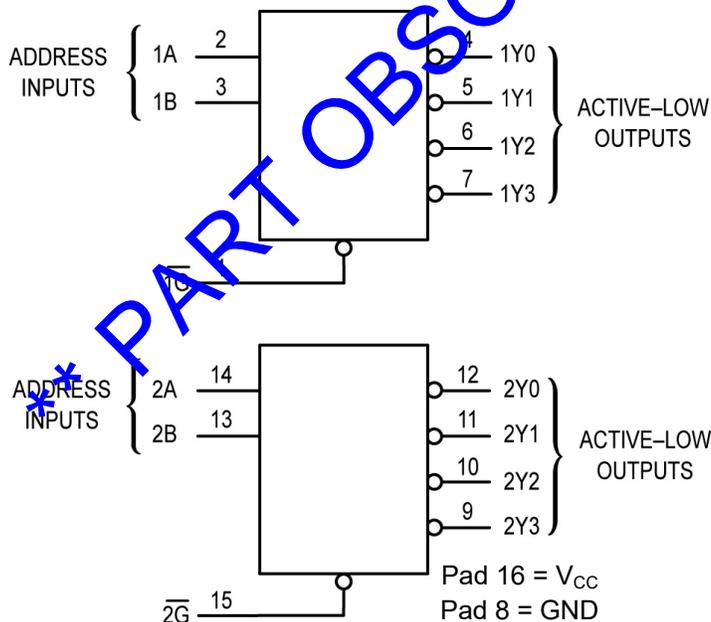
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1G}$	0.100	0.487
2	1A	0.100	0.150
3	1B	0.440	0.100
4	1Y3	0.640	0.100
5	1Y2	0.835	0.100
6	1Y1	1.030	0.100
7	1Y0	1.180	0.440
8	GND	1.180	0.720
9	GND	1.180	0.880
10	2Y3	1.180	1.190
11	2Y2	1.120	1.530
12	2Y1	0.826	1.530
13	2Y0	0.630	1.530
14	2B	0.436	1.530
15	2A	0.100	1.530
16	$\overline{2G}$	0.100	1.260
16	V <sub>CC</sub>	0.100	0.895
16	V <sub>CC</sub>	0.100	0.735

CONNECT CHIP BACK TO V<sub>CC</sub> OR FLOAT

## Logic Diagram



## Truth Table

INPUTS			OUTPUTS			
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care





## Pad Description

### ADDRESS INPUTS

1A, 1B, 2A, 2B

(Pads 2, 3, 14, 13)

When the respective 1-of-4 decoder is enabled these inputs determine which of its four active-low outputs is selected.

### CONTROL INPUTS

1G, 2G

(Pads 1, 15)

Active-low select inputs. For a low level on this input, the outputs for that particular decoder follow the address inputs. A high level on this input forces all outputs to a high level.

### OUTPUTS

1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3

(Pads 4-7, 12, 11, 10, 9)

Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current, per pin	$I_{IN}$	±20	mA
DC Output Current, per pin	$I_{OUT}$	±50	mA
DC $V_{CC}$ or GND Current, per pin	$I_{CC}$	±50	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	$V_{CC}$	2	6	V	
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V	
Operating Temperature Range	$T_J$	-55	+125	°C	
Output Current – High	$I_{OH}$	-	-24	mA	
Output Current – Low	$I_{OL}$	-	24	mA	
Input Rise and Fall Time ( $V_{IN}$ from 30% to 70%)	$t_r, t_f$	$V_{CC} = 3.0V$	0	150	ns/V
		$V_{CC} = 4.5V$	0	40	
		$V_{CC} = 5.5V$	0	24	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.





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## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	V <sub>IH</sub>	3.0V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>OUT</sub>   ≤ 20μA	2.1	2.1	2.1	V
		4.5V		3.15	3.15	3.15	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V <sub>IL</sub>	3.0V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>OUT</sub>   ≤ 20μA	0.9	0.9	0.9	V
		4.5V		1.35	1.35	1.35	
		5.5V		1.65	1.65	1.65	
Minimum High-Level Output Voltage	V <sub>OH</sub>	3.0V	I <sub>OUT</sub> = -50μA	2.9	2.9	2.9	V
		4.5V		4.4	4.4	4.4	
		5.5V		5.4	5.4	5.4	
	3.0V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -12 mA	2.56	2.46	2.40		
	4.5V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24mA <sup>5</sup>	3.83	3.76	3.70		
	5.5V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24mA <sup>5</sup>	4.86	4.76	4.70		
	5.5V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -50mA <sup>6</sup>	-	-	3.85		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	3.0V	I <sub>OUT</sub> = 50μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		5.5V		0.1	0.1	0.1	
		3.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 12mA	0.36	0.44	0.5	
		4.5V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 24mA <sup>5</sup>	0.36	0.44	0.5	
		5.5V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 24mA <sup>5</sup>	0.36	0.44	0.5	
		5.5V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   50mA <sup>6</sup>	-	-	1.65	
Maximum Input Leakage Current	I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Minimum Dynamic Output Current <sup>7</sup>	I <sub>OLD</sub>	5.5V	V <sub>OLD</sub> = 1.65V Max	-	75	50	mA
	I <sub>OHD</sub>	5.5V	V <sub>OHD</sub> = 3.85V Min	-	-75	-50	
Maximum Quiescent Supply Current	I <sub>CC</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0μA	8	80	160	μA

4. -55°C ≤ T<sub>J</sub> ≤ +125°C 5. All outputs loaded; thresholds on input associated with output under test. 6. Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C 7. Maximum test duration 2ms, one output loaded at a time





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## AC Electrical Characteristics<sup>8</sup> ( $V_{CC} 3.3V \pm 0.3V, V_{CC} 5V \pm 0.3V$ )

PARAMETER	SYMBOL	$V_{CC}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, A or B to Y (Figure 1,3)	$t_{PLH}$	3.3V	$C_L = 50pF, t_r = t_f = 3ns$	11.5	13	14.7	ns
		5.0V		8.5	9.5	10.5	
	$t_{PHL}$	3.3V	$C_L = 50pF, t_r = t_f = 3ns$	10	11	14.7	ns
		5.0V		7.5	8.5	10.5	
Maximum Propagation Delay, G to Y (Figure 2,3)	$t_{PLH}$	3.3V	$C_L = 50pF, t_r = t_f = 3ns$	12	13	14.7	ns
		5.0V		8.5	10	10.5	
	$t_{PHL}$	3.3V	$C_L = 50pF, t_r = t_f = 3ns$	10	11	14.7	ns
		5.0V		7.5	8.5	10.5	
Maximum Input Capacitance	$C_{IN}$	-	-	4.5	4.5	4.5	pF
Power Dissipation Capacitance (Per Decoder) <sup>9</sup>	$C_{PD}$	-	$T_J = 25^\circ C, V_{CC} = 5.0V$	TYPICAL			
				40			pF

8. Not production tested in die form, characterized by chip design and tested in package.

9. Used to determine the no-load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

### Switching Waveforms

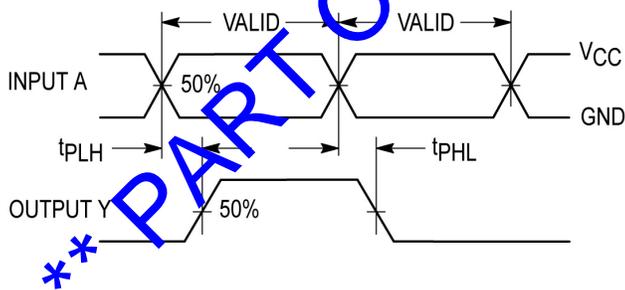


Figure 1 – Propagation Delay & Timing, Input to Output

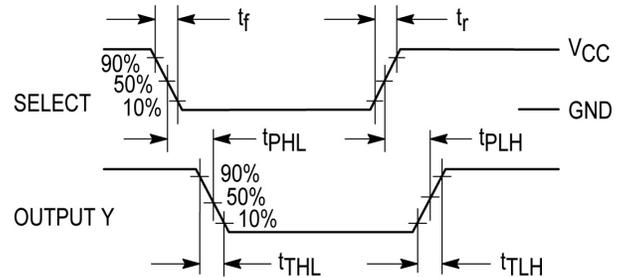
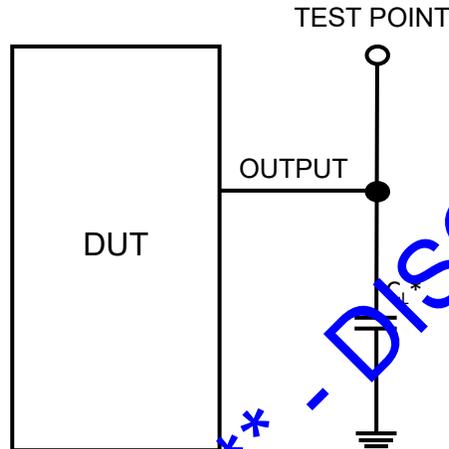


Figure 2 – Propagation Delay & Timing, Input Select to Output





## Test Circuit



\* Includes all probe and jig capacitance

Figure 3 – Test Circuit

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