



Bipolar TTL Logic – 5406

High Voltage Hex Inverter Buffer / Driver Logic IC in bare die form

Rev 1.0
29/07/20

Description

The 5406 comprises x6 inverter buffer/drivers with high voltage open-collector outputs. The device finds use as high-level circuit interface or for driving high-current loads and is also characterised to drive TTL inputs as inverted buffer. The device has a 30V minimum breakdown voltage and 30mA maximum sink current.

Features:

- High Sink-Current Capability: 30mA
- High Voltage Open-Collector Driver
- Minimum breakdown voltage: 30V
- Input Clamp Diodes minimize transmission-line effects
- TTL compatible inputs
- Direct drop-in replacement for obsolete components in long term programs

Ordering Information

The following part suffixes apply:

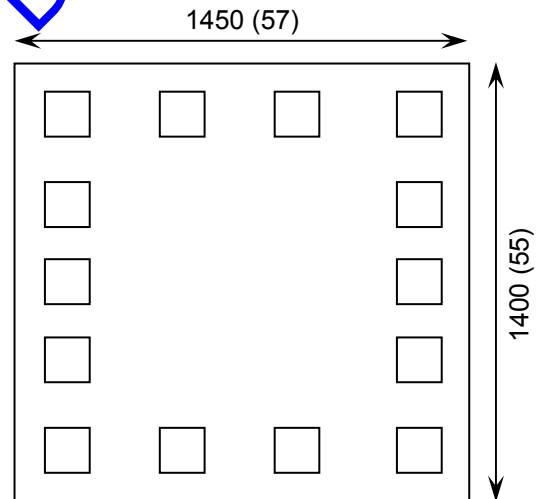
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in μm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- ~~Sawn Wafer on Tape~~ – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350 μm (14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

| | | |
|------------------------|--|-----------------------|
| Die Size (Unsawn) | 1450 x 1400 57 x 55 | μm mils |
| Minimum Bond Pad Size | 140 x 140 5.5 x 5.5 | μm mils |
| Die Thickness | 350 (± 20) 13.78 (± 0.79) | μm mils |
| Top Metal Composition | Al 1%Si 1.1 μm | |
| Back Metal Composition | N/A – Bare Si | |

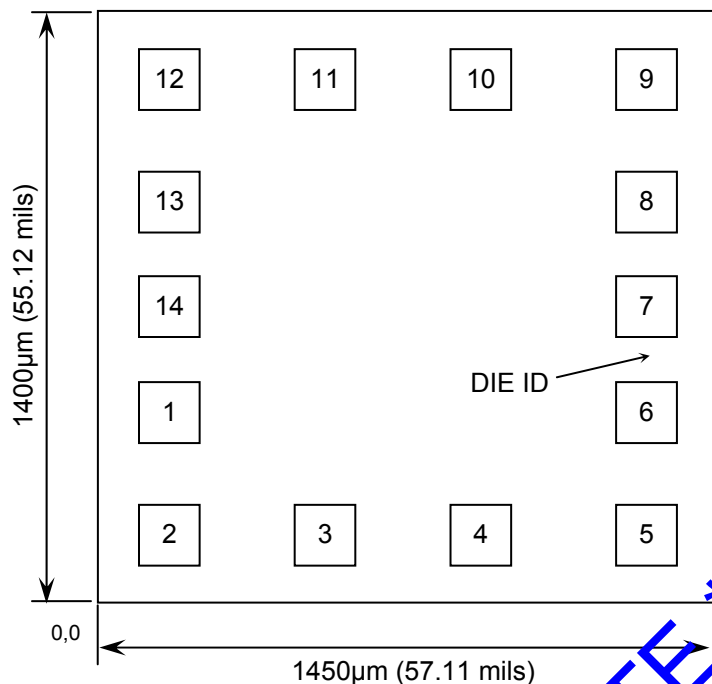




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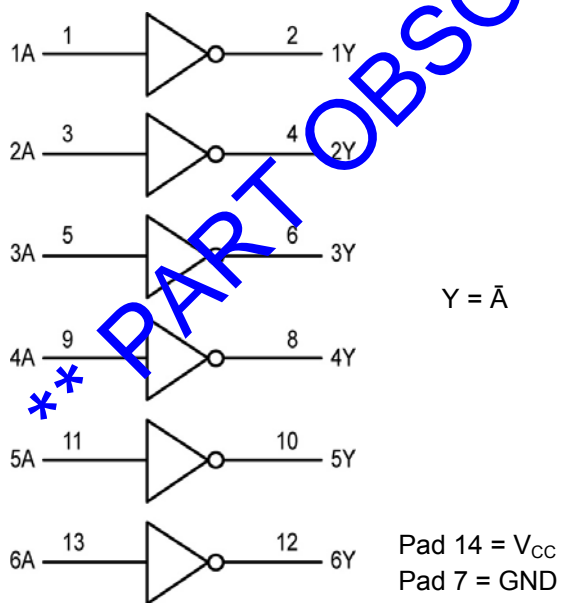
Pad Layout and Functions



| PAD | FUNCTION | COORDINATES (mm) | |
|-----|-----------------|------------------|-------|
| | | X | Y |
| 1 | 1A | 0.090 | 0.380 |
| 2 | 1Y | 0.090 | 0.090 |
| 3 | 2A | 0.460 | 0.090 |
| 4 | 2Y | 0.830 | 0.090 |
| 5 | 3A | 1.220 | 0.090 |
| 6 | 3Y | 1.220 | 0.380 |
| 7 | GND | 1.220 | 0.630 |
| 8 | 4Y | 1.220 | 0.880 |
| 9 | 4A | 1.220 | 1.170 |
| 10 | 5Y | 0.830 | 1.170 |
| 11 | 5A | 0.460 | 1.170 |
| 12 | 6Y | 0.090 | 1.170 |
| 13 | 6A | 0.090 | 0.880 |
| 14 | V _{CC} | 0.090 | 0.630 |

CONNECT CHIP BACK TO GND OR FLOAT

Logic Diagram



Truth Table

| INPUTS | | OUTPUT |
|--------|--|--------|
| A | | Y |
| L | | Z |
| H | | L |

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance





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Absolute Maximum Ratings¹

| PARAMETER | SYMBOL | VALUE | UNIT |
|---------------------------|-----------|------------|------|
| DC Supply Voltage | V_{CC} | 7.0 | V |
| DC Input Voltage | V_{IN} | 5.5 | V |
| DC Output Voltage | V_{OUT} | 30 | V |
| Storage Temperature Range | T_{STG} | -65 to 150 | °C |

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|-----------------------------|----------|------|------|-------|
| Supply Voltage | V_{CC} | 4.5 | 5.5 | V |
| High-Level Input Voltage | V_{IH} | 2 | - | V |
| Low-Level Input Voltage | V_{IL} | - | 0.8 | V |
| High-Level Output Voltage | V_{OH} | - | 30 | V |
| Low-Level Output Current | I_{OL} | - | 30 | mA |
| Operating Temperature Range | T_J | *-55 | +125 | °C |

DC Electrical Characteristics² $T_J = -55^{\circ}\text{C}$ to 125°C unless otherwise specified

| PARAMETER | SYMBOL | CONDITIONS | LIMITS | | | UNITS |
|---------------------------|----------|---|--------|-----|------|-------|
| | | | MIN | TYP | MAX | |
| Input Clamp Voltage | V_{IK} | $V_{CC} = 4.5\text{V}, I_{IN} = -12\text{mA}$ | - | - | -1.5 | V |
| High-Level Output Current | I_{OH} | $V_{CC} = 4.5\text{V}, V_{IL} = 0.8\text{V}, V_{OH} = 30\text{V}$ | - | - | 0.25 | mA |
| Low-Level Output Voltage | V_{OL} | $V_{CC} = 4.5\text{V}, V_{IH} = 2\text{V}, I_{OL} = 16\text{mA}$ | - | - | 0.4 | V |
| | | $V_{CC} = 4.5\text{V}, V_{IH} = 2\text{V}, I_{OL} = 30\text{mA}$ | - | - | 0.7 | |
| Input Current | I_{IN} | $V_{CC} = 5.5\text{V}, V_{IN} = 5.5\text{V}$ | - | - | 1 | mA |
| High-Level Input Current | I_{IH} | $V_{CC} = 5.5\text{V}, V_{IH} = 2.4\text{V}$ | - | - | 0.04 | mA |
| Low-Level Input Current | I_{IL} | $V_{CC} = 5.5\text{V}, V_{IL} = 0.4\text{V}$ | - | - | -1.6 | mA |
| Supply Current | I_{CC} | $V_{CC} = 5.5, \text{Output High}$ | - | - | 48 | mA |
| | | $V_{CC} = 5.5, \text{Output Low}$ | - | - | 51 | |





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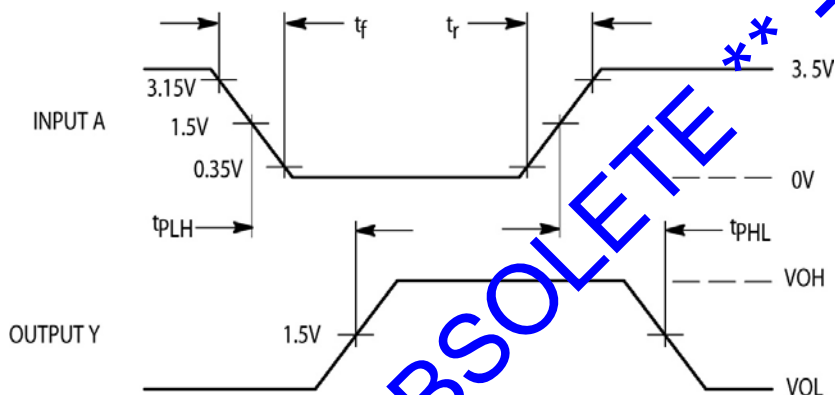
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AC Electrical Characteristics²

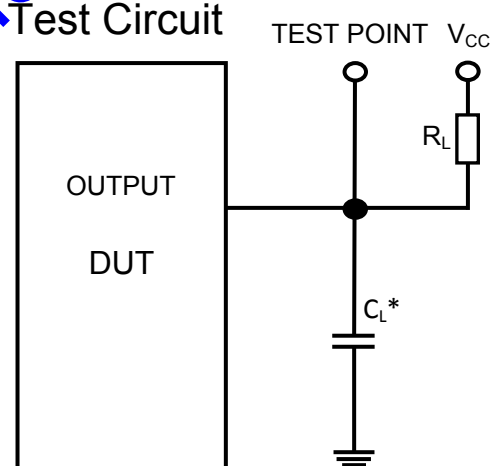
| PARAMETER | SYMBOL | CONDITIONS | LIMITS | | | UNITS |
|------------------------------------|-----------|--|--------|-----|-----|-------|
| | | | MIN | TYP | MAX | |
| Turn-Off Delay, Input to Output | t_{PLH} | $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $R_L = 110\Omega$, $C_L = 15\text{pF}$, Input $t_r = t_f = 10\text{ns}$ | - | - | 18 | ns |
| Turn-On Delay, Input to Output | t_{PHL} | | - | - | 20 | |

2. Not production tested in die form, characterized by chip design

Switching Waveform



Test Circuit



* Includes all probe and jig capacitance

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