

INN650N190A

1. General description

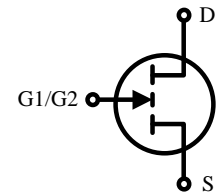
650V GaN-on-Silicon Enhancement-mode Power Transistor Bare Die

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications

- DCM/BCM PFC
- AHB/LLC/QR Flyback/ACF DCDC converter
- LED driver
- Fast battery charger
- Notebook/AIO adaptor
- Desktop PC/ATX/TV/power tool power supply



4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$ @ $V_{GS} = 6\text{ V}$	190	m Ω
$Q_{G,typ}$ @ $V_{DS} = 400\text{ V}$	2.8	nC
$I_{D,pulse}$	20.5	A
Q_{OSS} @ $V_{DS} = 400\text{ V}$	24.5	nC
Q_{rr} @ $V_{DS} = 400\text{ V}$	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Source
G1,G2	D	S

Table 3 Ordering information

Type/Ordering Code	Product Code
INN650N190A	INN650N190A
To order bare die form please contact sales@diedevices.com	

Table of contents

1. General description	1
2. Features	1
3. Applications.....	1
4. Key performance parameters.....	1
5. Pin information	1
6. Maximum ratings.....	3
7. Electric characteristics	4
8. Electric characteristics diagrams	6
9. Chip drawing	12
10.Revision history	13

6. Maximum ratings

at $T_j = 25\text{ °C}$ unless otherwise specified

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscence sales office

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	650	V	$V_{GS} = 0\text{ V}$, $T_j = -55\text{ °C}$ to 150 °C
Drain source voltage transient ¹	$V_{DS,transient}$	800	V	$V_{GS} = 0\text{ V}$
Drain source voltage, pulsed ²	$V_{DS,pulse}$	750	V	$T_j = 25\text{ °C}$; total time < 10 h
				$T_j = 125\text{ °C}$; total time < 1 h
Continuous current, drain source ³	I_D	11.5	A	$T_c = 25\text{ °C}$
Pulsed current, drain source ⁴	$I_{D,pulse}$	20.5	A	$T_c = 25\text{ °C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Pulsed current, drain source ⁴	$I_{D,pulse}$	11.5	A	$T_c = 125\text{ °C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Gate source voltage, continuous ⁵	V_{GS}	-1.4 to +7	V	$T_j = -55\text{ °C}$ to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	$T_j = -55\text{ °C}$ to 150 °C ; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$; open drain
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1 $V_{DS,transient}$ is intended for non-repetitive events, $t_{PULSE} < 200\text{ }\mu\text{s}$

2 $V_{DS,pulse}$ is intended for repetitive pulse, $t_{PULSE} < 100\text{ ns}$

3 Limited by maximum temperature allowed with the parts assembled in DFN 5X6 package

4 Limit was extracted from characterization test, not measured during production

5 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Electric characteristics¹

at $T_j = 25\text{ °C}$, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	$I_D = 12.2\text{ mA}; V_{DS} = V_{GS}; T_j = 25\text{ °C}$
		-	1.7	-		$I_D = 12.2\text{ mA}; V_{DS} = V_{GS}; T_j = 150\text{ °C}$
Drain-source leakage current	I_{DSS}	-	0.45	20	μA	$V_{DS} = 650\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$
		-	6	-		$V_{DS} = 650\text{ V}; V_{GS} = 0\text{ V}; T_j = 150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	60	-	μA	$V_{GS} = 6\text{ V}; V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	138	190	m Ω	$V_{GS} = 6\text{ V}; I_D = 3.9\text{ A}; T_j = 25\text{ °C}$
		-	300	-		$V_{GS} = 6\text{ V}; I_D = 3.9\text{ A}; T_j = 150\text{ °C}$
Gate resistance-G1 ²	R_{G1}	-	5	-	Ω	$f = 5\text{ MHz};$ open drain
Gate resistance-G2 ²	R_{G2}	-	6	-	Ω	$f = 5\text{ MHz};$ open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	96	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	30	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Reverse transfer Capacitance	C_{riss}	-	0.5	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Effective output capacitance, energy related ³	$C_{o(er)}$	-	43	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ⁴	$C_{o(tr)}$	-	60	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	24.5	-	nC	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	1.4	-	nS	$V_{DS} = 400\text{ V}; I_D = 8\text{ A}; L = 318\text{ }\mu\text{H};$ $V_{GS} = 6\text{ V}; R_{on} = 10\text{ }\Omega; R_{off} = 2\text{ }\Omega;$ See Figure 22
Turn-off delay time	$t_{d(off)}$	-	1.7	-	nS	
Rise time	t_r	-	4.0	-	nS	
Fall time	t_f	-	4.0	-	nS	
Output Capacitance Stored Energy	E_{oss}	-	3.5	-	μJ	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$

1 The electrical characteristics parameters were tested with the parts assembled in DFN 5X6 package

2 Refer to chip drawing section, device owns different R_G while bonding from different gate pad

3 $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

4 $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 7 Gate charge characteristics

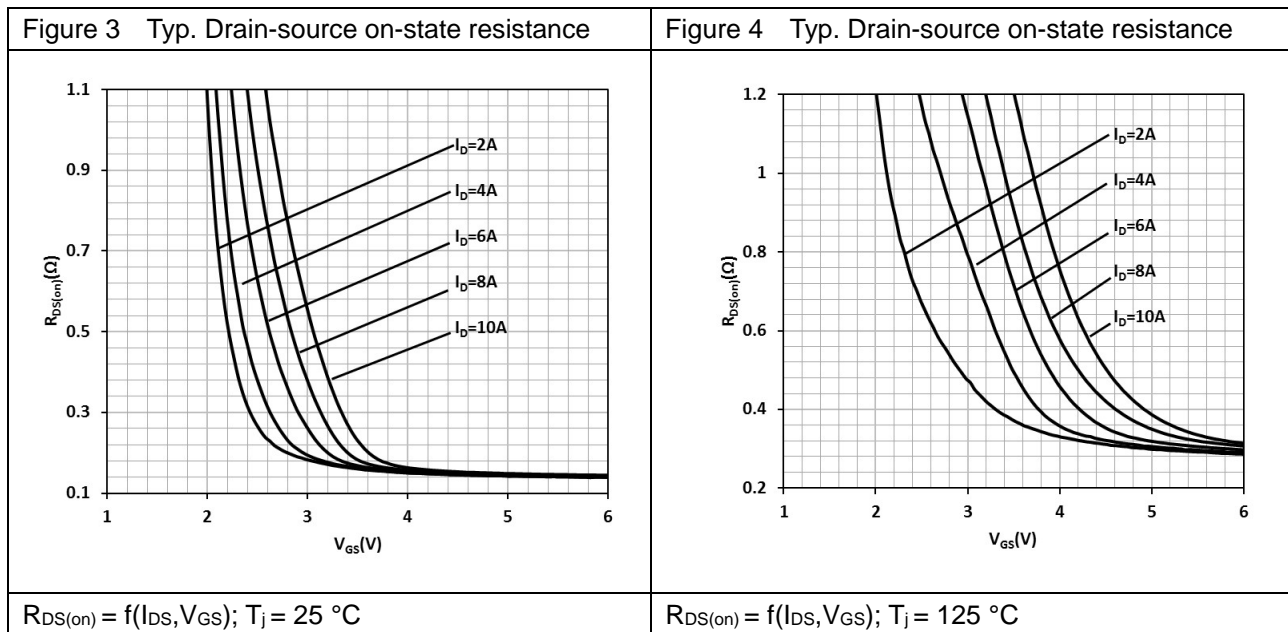
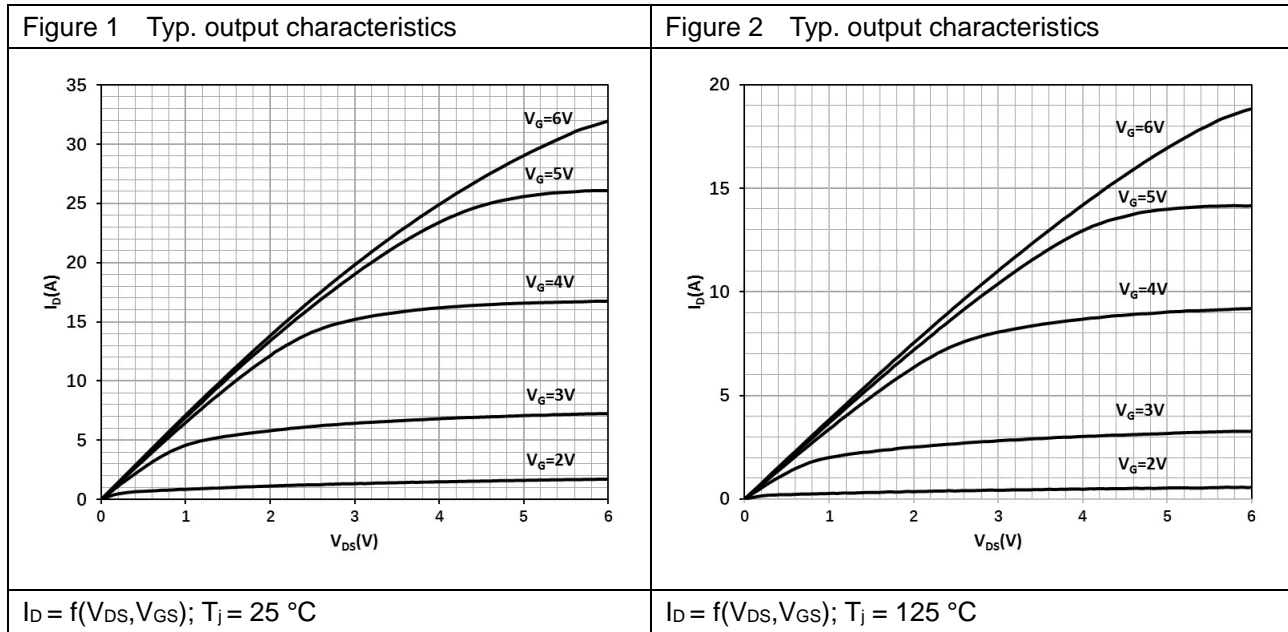
Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2.8	-	nC	$V_{GS} = 0$ to 6 V; $V_{DS} = 400$ V; $I_D = 3.9$ A
Gate-source charge	Q_{GS}	-	0.25	-	nC	
Gate-drain charge	Q_{GD}	-	1.1	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.2	-	V	$V_{DS} = 400$ V; $I_D = 3.9$ A

Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.6	-	V	$V_{GS} = 0$ V; $I_S = 3.9$ A
Pulsed current, reverse	$I_{S,pulse}$	-	-	20.5	A	$V_{GS} = 6$ V; $t_{PULSE} = 10$ μ s
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_S = 3.9$ A; $V_{DS} = 400$ V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

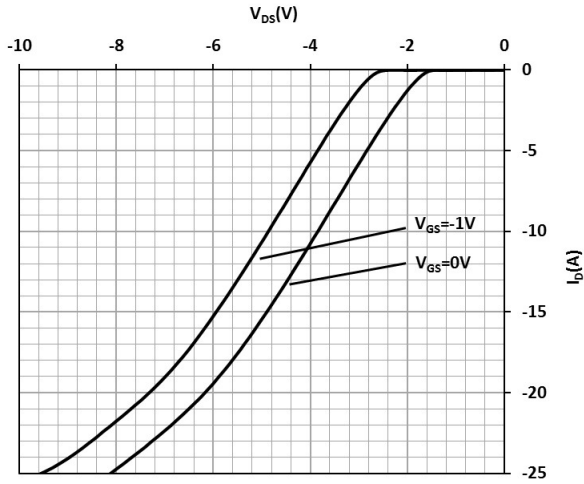
8. Electric characteristics diagrams¹

at $T_j = 25\text{ °C}$, unless specified otherwise



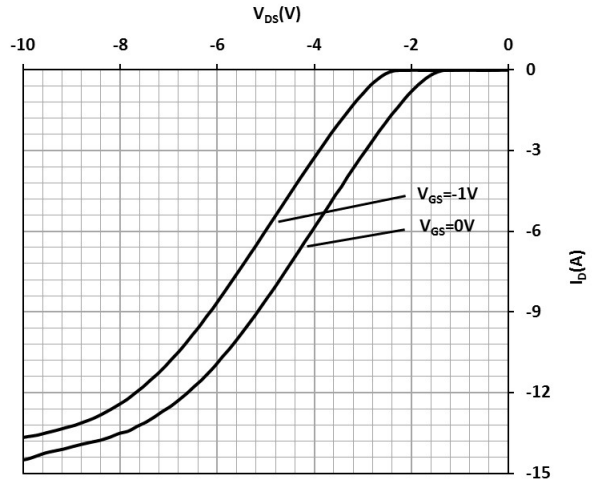
¹ The typical electrical characteristic curves were measured with the parts assembled in DFN 5X6 package.

Figure 5 Typ. channel reverse characteristics



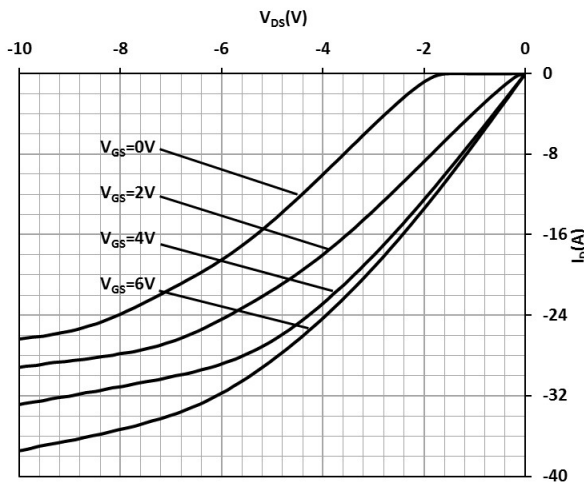
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^\circ\text{C}$

Figure 6 Typ. channel reverse characteristics



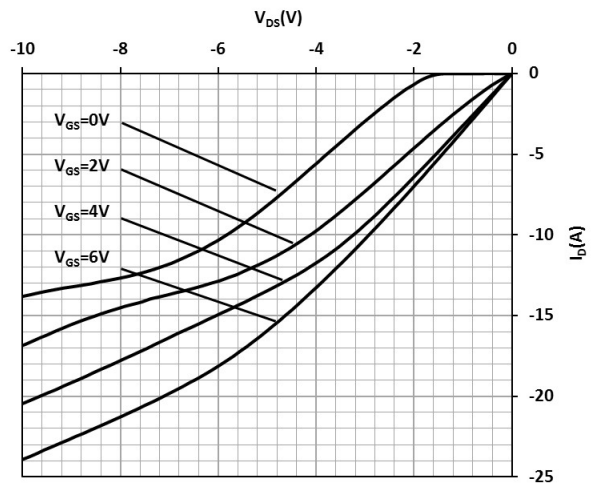
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^\circ\text{C}$

Figure 7 Typ. channel reverse characteristics



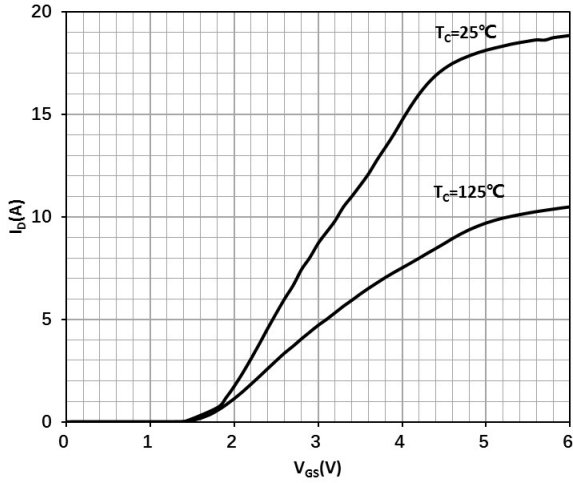
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^\circ\text{C}$

Figure 8 Typ. channel reverse characteristics



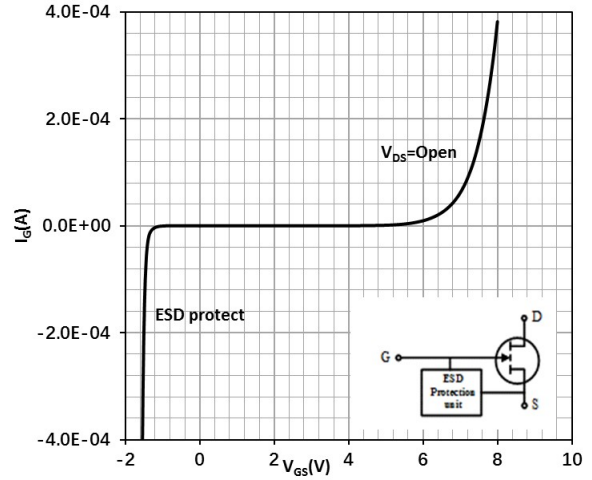
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^\circ\text{C}$

Figure 9 Typ. transfer characteristics



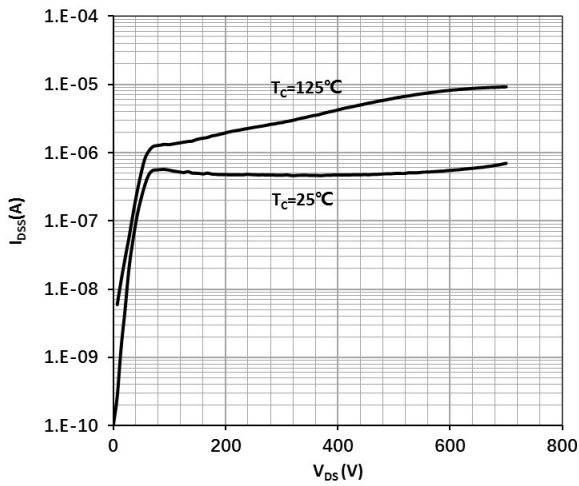
$I_D = f(V_{GS}); V_{DS} = 3 \text{ V}$

Figure 10 Typ. Gate-to-Source leakage



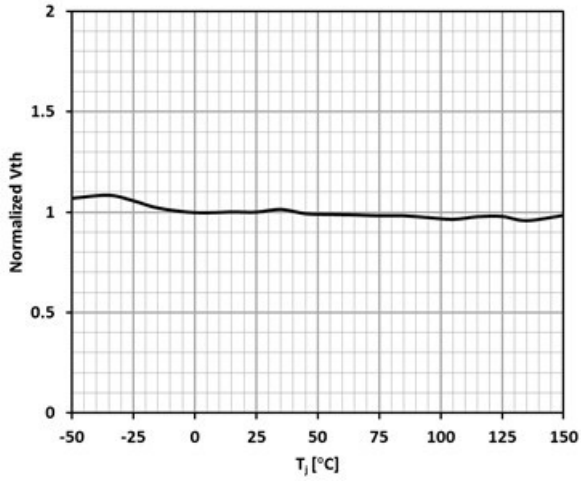
$I_G = f(V_{GS}); I_G$ reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



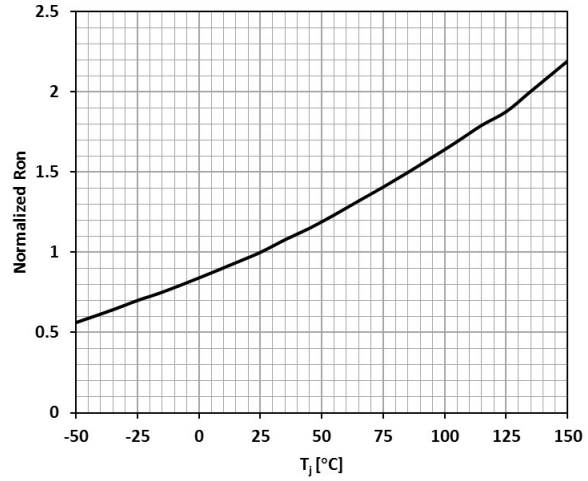
$I_{DSS} = f(V_{DS}); V_{GS} = 0 \text{ V}$

Figure 12 Gate threshold voltage



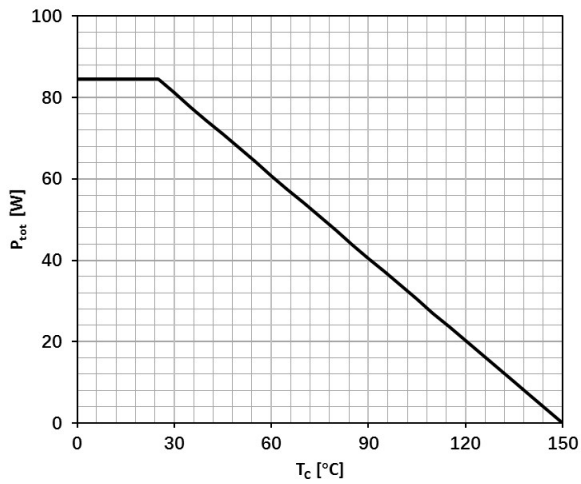
$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 12.2 \text{ mA}$

Figure 13 Drain-source on-state resistance



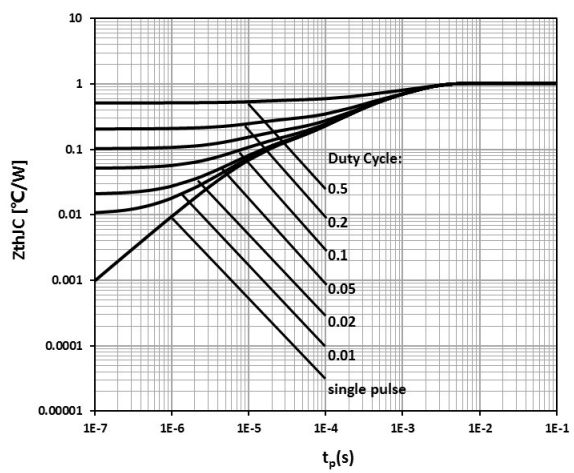
$R_{DS(on)} = f(T_j); I_D = 3.9 \text{ A}; V_{GS} = 6 \text{ V}$

Figure 14 Power dissipation



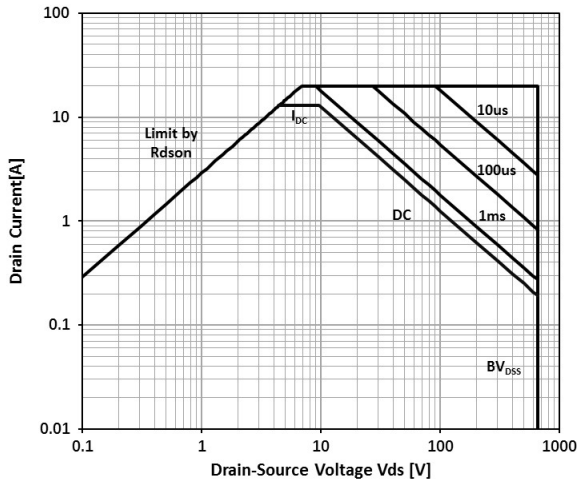
$P_{tot} = f(T_c)$

Figure 15 Max.transient thermal impedance



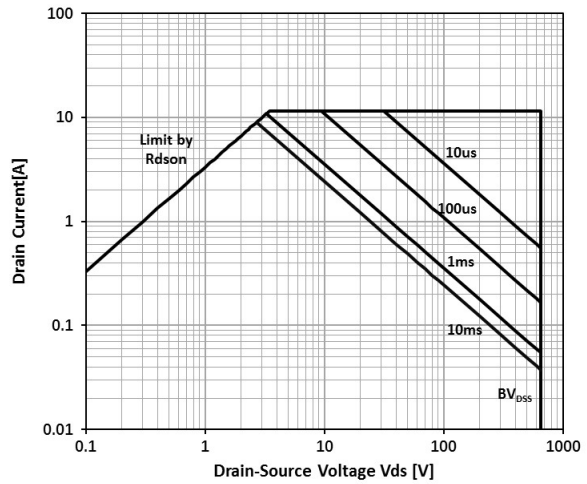
$Z_{thJC} = f(t_p, D)$

Figure 16 Safe operating area



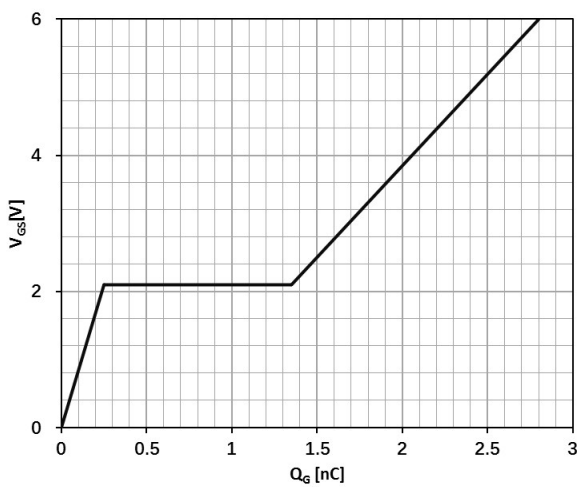
$I_D = f(V_{DS}); T_C = 25\text{ °C}$

Figure 17 Safe operating area



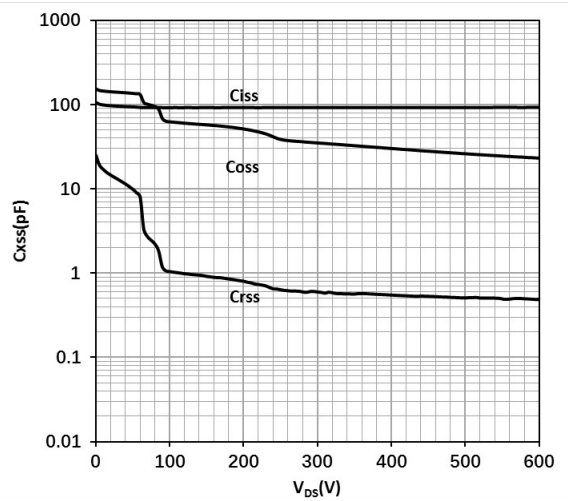
$I_D = f(V_{DS}); T_C = 125\text{ °C}$

Figure 18 Typ. gate charge



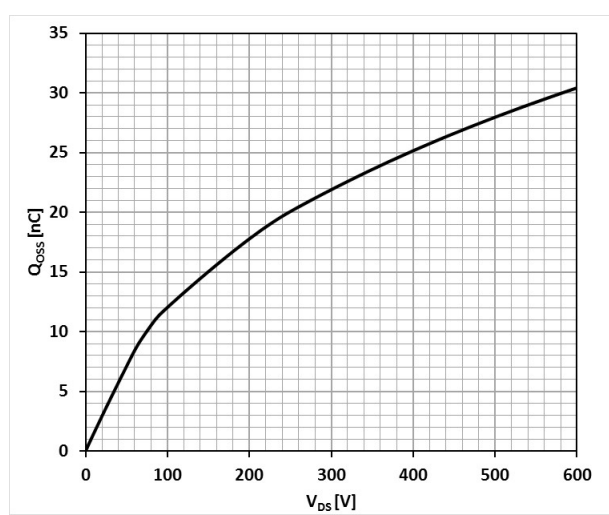
$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 5\text{ A}$

Figure 19 Typ. capacitances



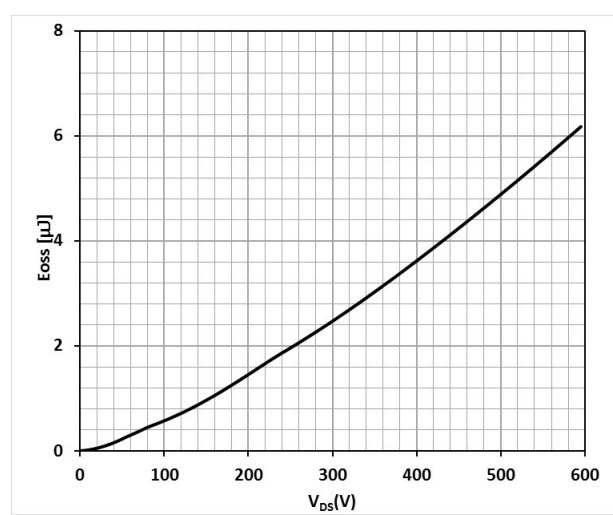
$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$

Figure 20 Typ. output charge



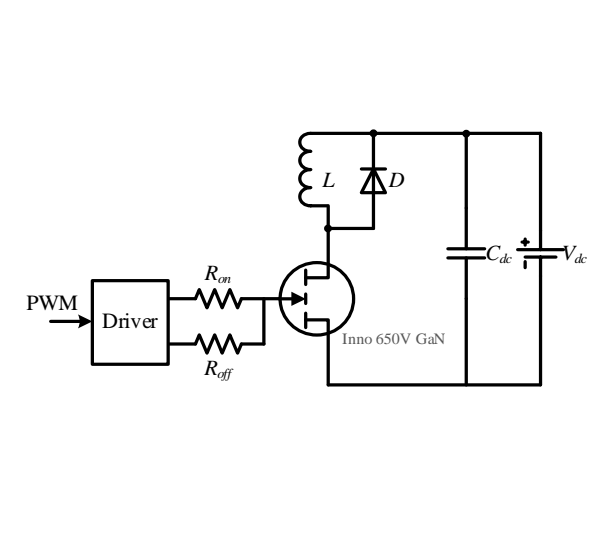
$Q_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 21 Typ. Coss stored Energy



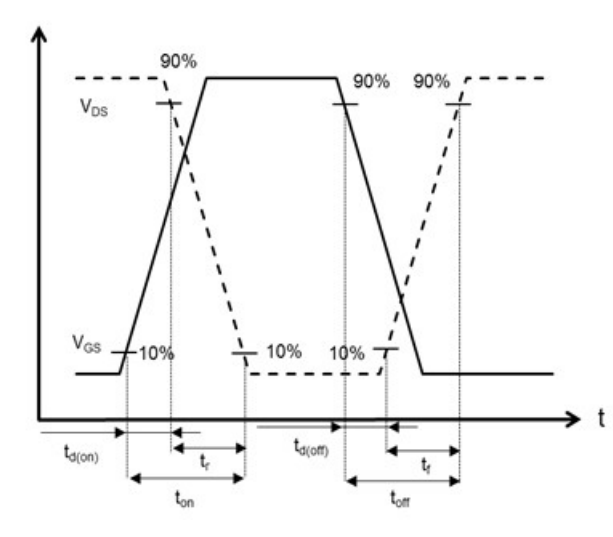
$E_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 22 Typ. Switching times with inductive load

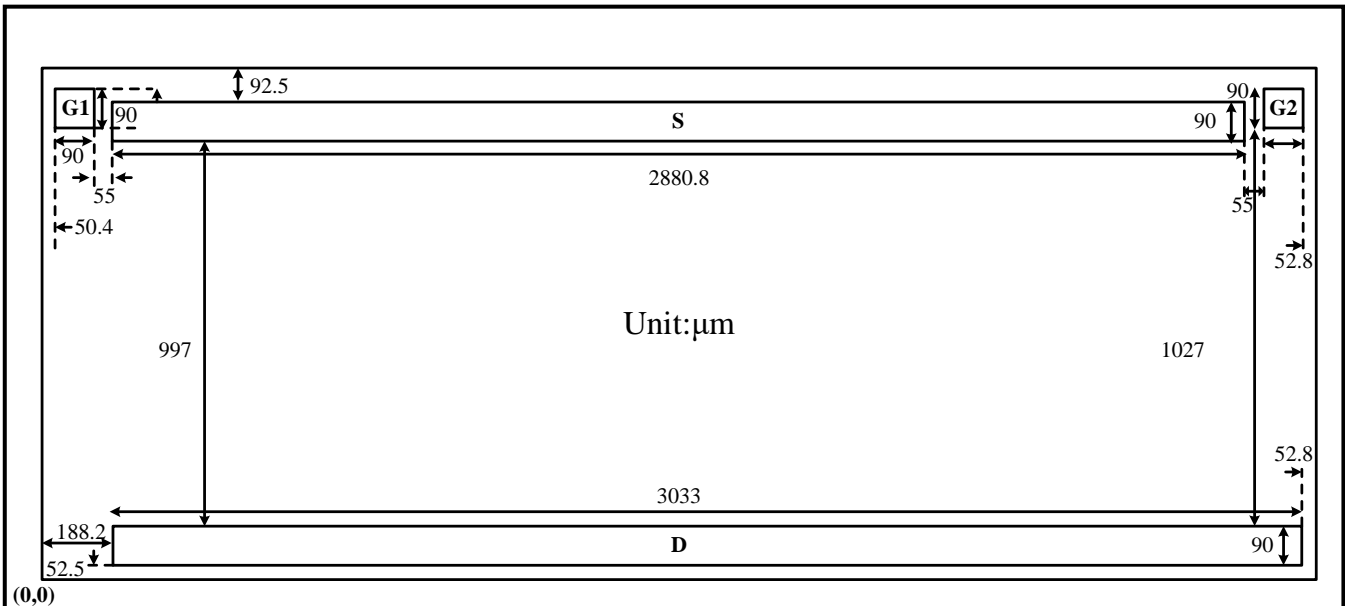


$V_{DS} = 400 \text{ V}, I_D = 8 \text{ A}, L = 318 \text{ } \mu\text{H}, V_{GS} = 6 \text{ V},$
 $R_{on} = 10 \text{ } \Omega, R_{off} = 2 \text{ } \Omega$

Figure 23 Typ. Switching times waveform



9. Chip drawing



Wafer features

Physical Characteristics		Unit
Wafer Size	8	inches
Wafer Thickness	1150	μm
Die Size (with S/L)	3.35 x 1.4	mm^2
Scribe Street Width	80	μm
Top Metal Materials	Al-Cu	
Top Metal thickness	3.5	μm
Passivation Materials	SiN, SiO ₂	
Passivation Thickness	2.1	μm
PI Materials	Polyimide	
PI Thickness	10	μm
Gate Pad Size	G1: 90 x 90 G2: 90 x 90	μm^2
Source Pad Size	2280.8 x 90	μm^2
Drain Pad Size	3033 x 90	μm^2
TGV	No	
Backside	Silicon	

Note: All the pad size refers to PI top opening size, actual size at PI bottom (top metal exposure) is about 4~8 μm shorter than top opening.

10. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-04-22	1.0 version release

Important Notice

The information provided in this document is intended as a guide only and shall not in any event be regarded as a guarantee of conditions, characteristics or performance. Innoscience does not assume any liability arising out of the application or use of any product described herein, including but not limited to any personal injury, death, or property or environmental damage. No licenses, patent rights, or any other intellectual property rights is granted or conveyed. Innoscience reserves the right to modify without notice. All rights reserved.