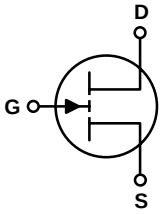
INN100W070A

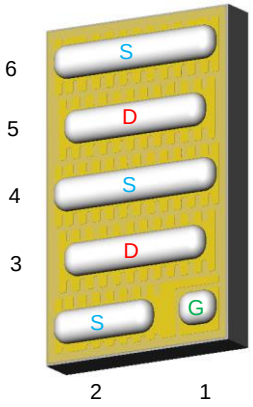
1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in Solder Bar WLCSP with 2.50 mm x 1.50 mm package size.



2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small package size
- Zero reverse recovery charge



Bottom View

3. Applications

- Synchronous rectification
- Class-D audio
- High frequency DC-DC converter
- Communication base station
- Motor driver

4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	7	mΩ
$Q_{G,typ}$ @ V_{DS} = 50V	4.5	nC
$I_{DS,Continue}$	29	A
Q_{OSS}@ V_{DS} = 50V	25	nC

5. Pin information

Table 2 Pin information

PIN	Pin Description	Pin Function
2,4,6	Source	Power Source
3,5	Drain	Power Drain
1	Gate	Driver Gate

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100W070A	WLCSP 2.50x1.50	J19

Table of contents

6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous current	29	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	125	A
V_{GS}	Gate-to-Source Voltage	5.5	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.62	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.98	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]	62.76	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at T_j = 25 °C unless otherwise specified.

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	100	-	-	V	V_{GS} = 0 V, I_D = 600 μA
I_{DSS}	Drain Source Leakage	-	40	200	μA	V_{GS} = 0 V, V_{DS} =80 V
I_{GSS}	Gate-to-Source Forward Leakage(25°C)	-	10	200	μA	V_{GS} = 5 V
	Gate-to-Source Forward Leakage(125°C)		0.1	4	mA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage	-	30	20	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	V_{DS} = V_{GS}, I_D = 4.3 mA
$R_{DS(on)}$	Drain-Source On-state Resistance	-	5.5	7	mΩ	V_{GS} = 5 V, I_D = 16 A
V_{SD}	Source-Drain Forward Voltage	-	1.4	-	V	I_S = 0.5 A, V_{GS} = 0 V

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	485	776	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{OSS}	Output Capacitance	-	220	352		V_{GS} = 0 V, V_{DS} = 50 V
C_{RSS}	Reverse Transfer Capacitance	-	3.5	-		V_{GS} = 0 V, V_{DS} = 50 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	340	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	500	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
R_G	Gate resistance	-	1.7	-	Ω	
Q_G	Total Gate Charge	-	4.5	6.7	nC	V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 16 A
Q_{GS}	Gate to Source Charge	-	1	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D = 16 A
Q_{GD}	Gate to Drain Charge	-	0.8	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D = 16 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	0.6	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D = 16 A
Q_{OSS}	Output Charge	-	25	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V

9. Electric characteristics diagrams

at T_j = 25 °C unless otherwise specified.

Fig. 1 Typical Output Characteristics (T_J=25°C)

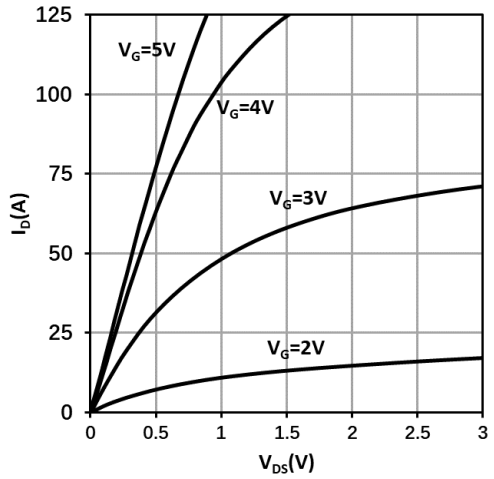


Fig. 2 Typical Output Characteristics (T_J=125°C)

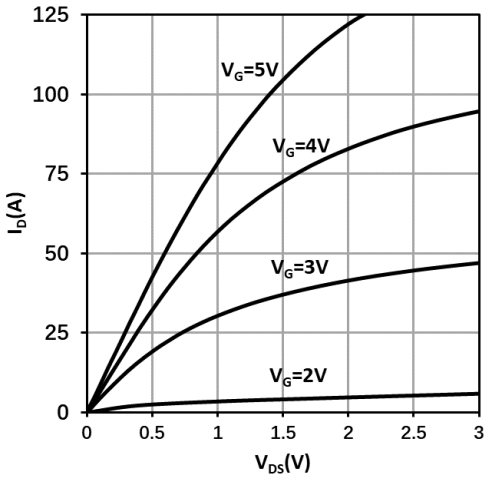


Fig. 3 Typical Drain On-state Resistance (T_J=25°C)

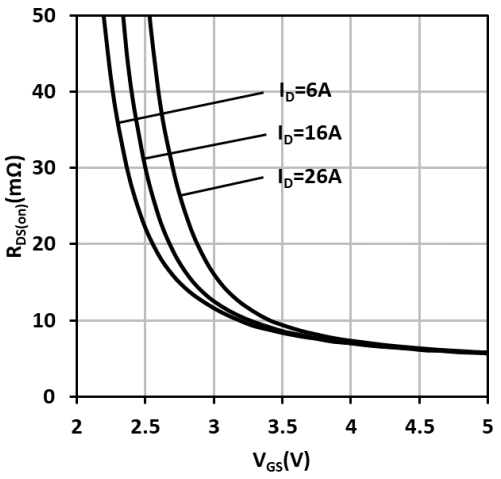


Fig. 4 Typical Drain On-state Resistance (T_J=125°C)

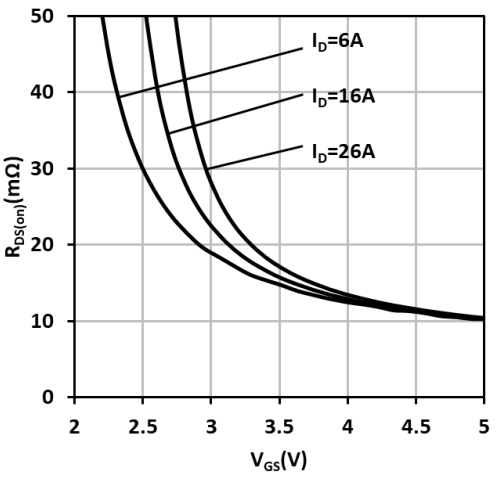


Fig. 5 Normalized On-State Resistance vs. Temp.

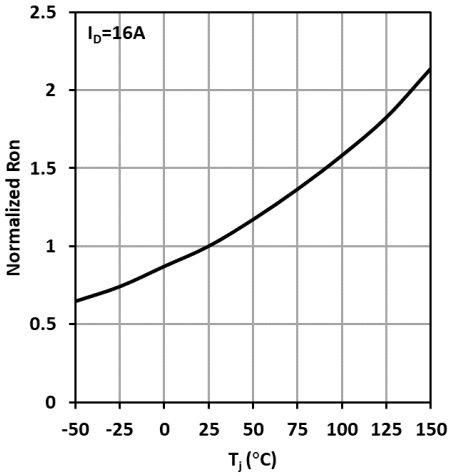


Fig. 6 Typical Transfer Characteristics

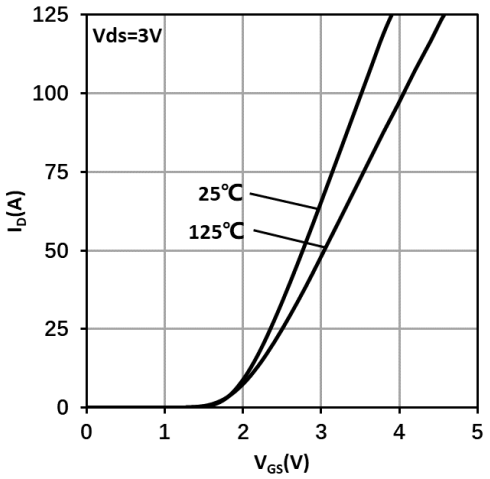


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0, T_J$=25°C)

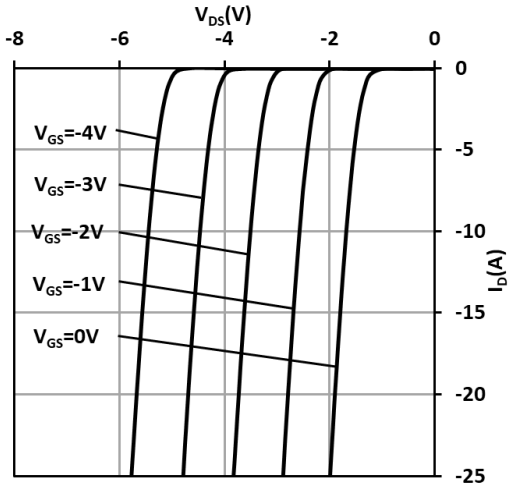


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0, T_J$=25°C)

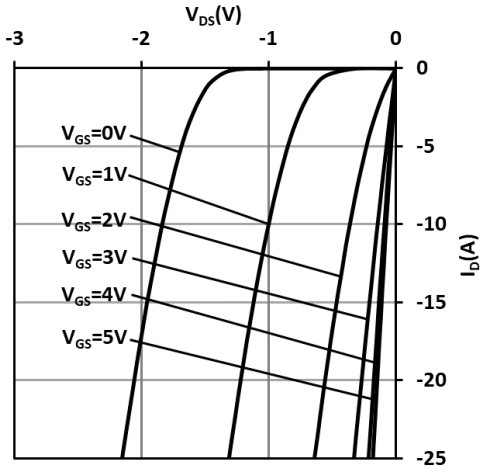


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0$, T_J=125°C)

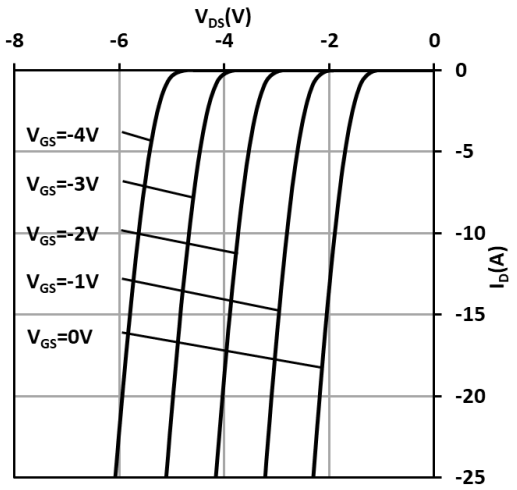


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0$, T_J=125°C)

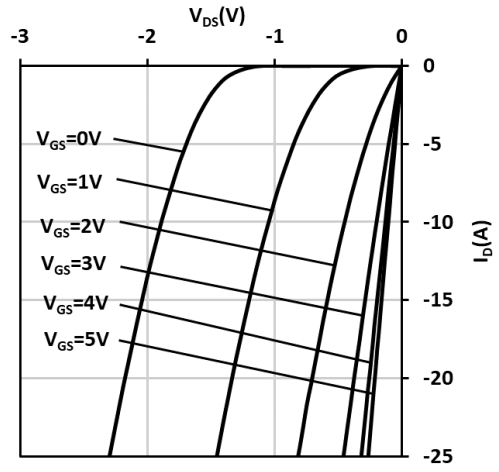


Fig. 11 Typ. Capacitances Characteristics

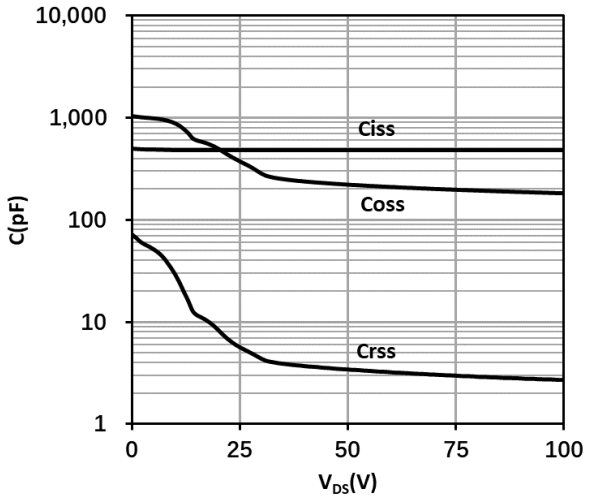


Fig. 12 Typ. Gate Charge

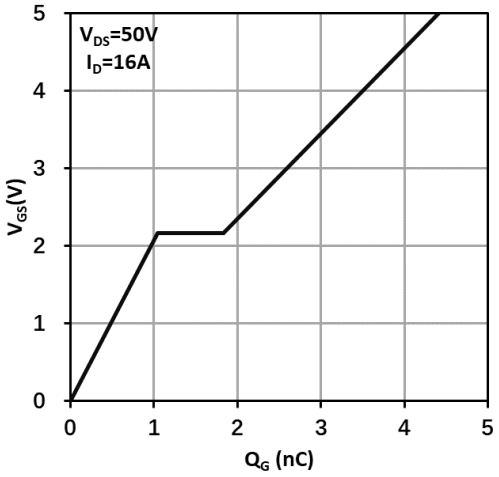


Fig. 13 Normalized Threshold Voltage vs. Temp.

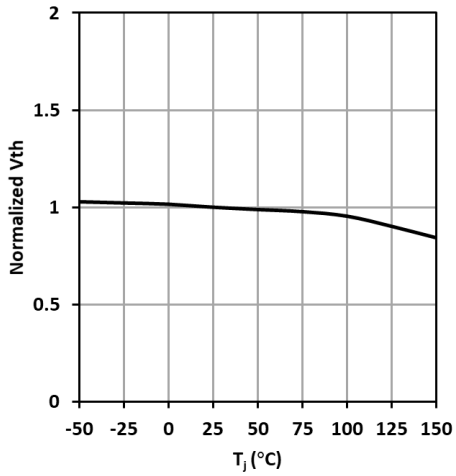


Fig. 14 Output Charge

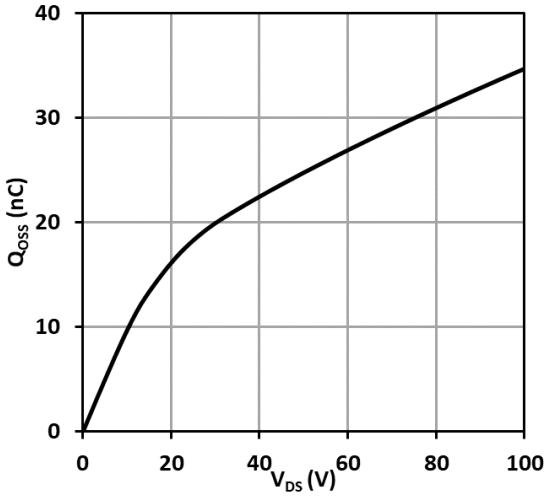


Fig. 15 Output Capacitance Stored Energy

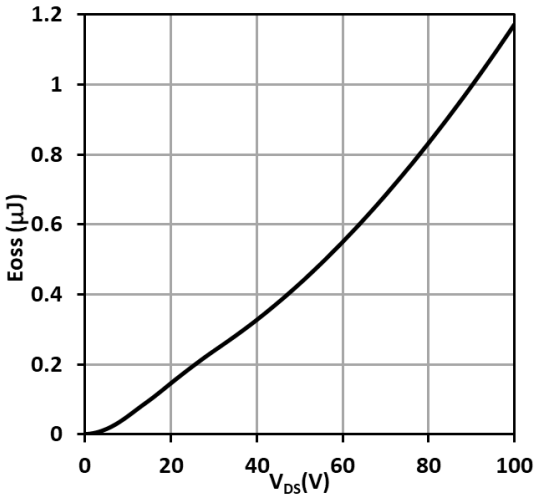


Fig. 16 Power Dissipation

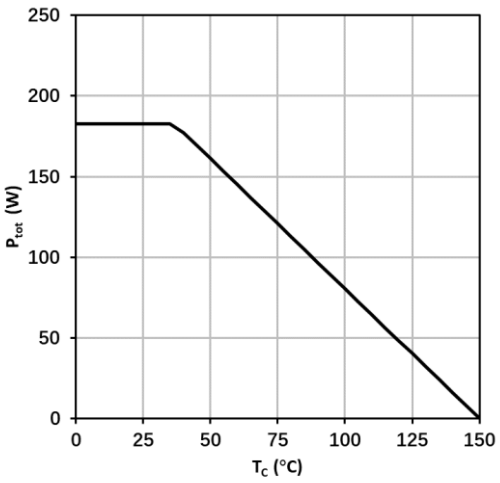


Fig. 17 Safe Operating Area

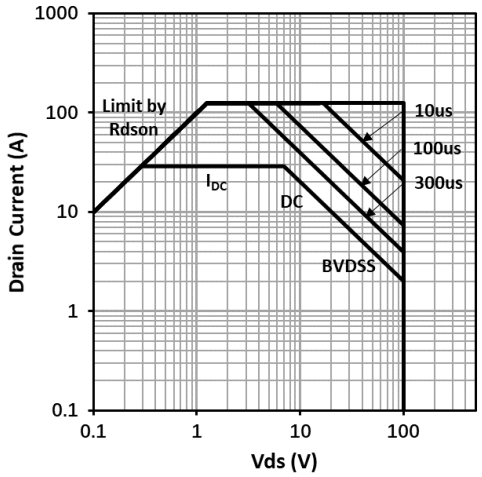
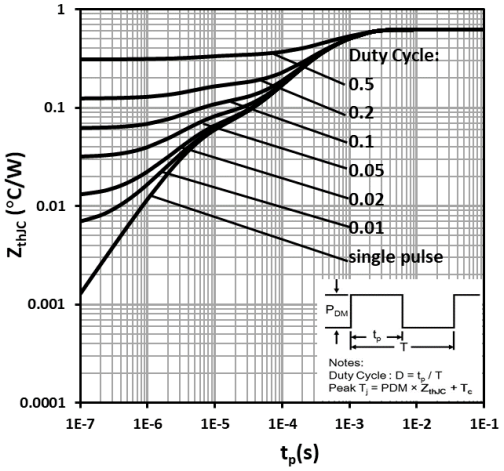
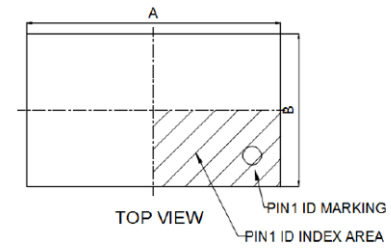


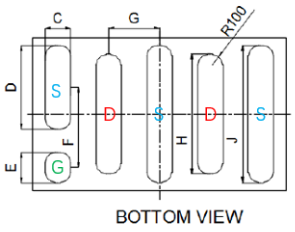
Fig. 18 Max. Transient Thermal Impedance



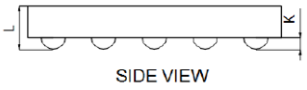
10. Package outlines

Package Reference



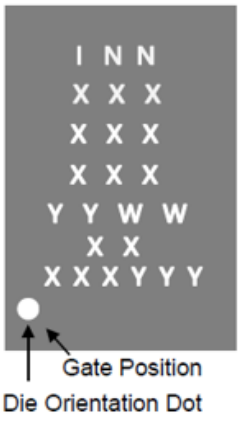


SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	2.475	2.5	2.525	
B	1.475	1.5	1.525	
C	0.23	0.25	0.27	6X
D	0.805	0.825	0.845	
E	0.28	0.3	0.32	
F	0.7875 BASIC			
G	0.5 BASIC			
H	1.155	1.175	1.195	2X
J	1.33	1.35	1.37	2X
K	0.1	0.12	0.14	
L	0.395	0.43	0.465	



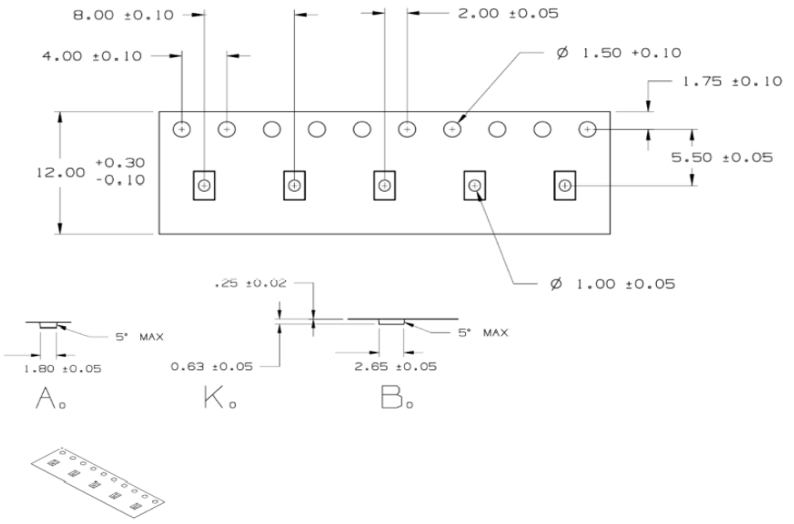
NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS SOLDER BAR VIEW.
3)COMPLIES WITH JEDEC MO-211.
4)DRAWING IS NOT TO SCALE.
5)A,B IS PACKAGE SIZE
6)BAR COPLANARITY SHALL BE 0.05 MILLMETERS MAX

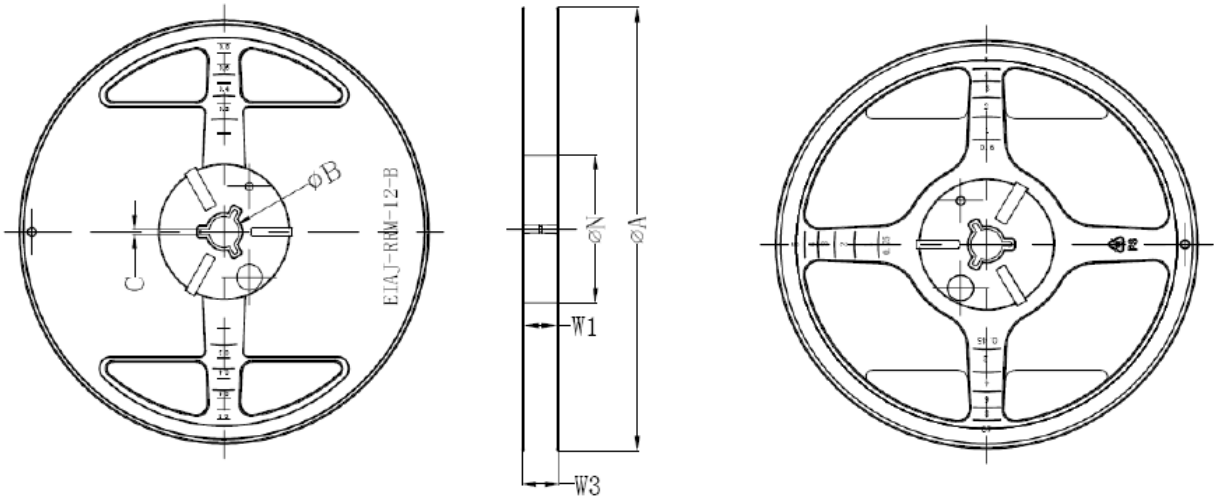
Marking Reference:



Row	Description	Example
Row1	Company name	INN
Row2	Product code	XXX
Row3	Lot Code	XXX
Row4		XXX
Row5	Date code	YYWW
Row6	Wafer ID	XX
Row7	Location ID	XXXYYY

11. Reel information



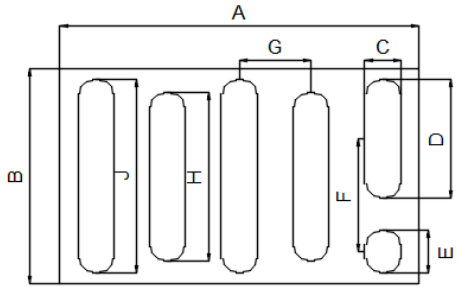


名称	øA	øN	øB	C	$W1^{+2}_{0}$	$W3^{+3}_{0}$
7X12	179^{+2}_{-2}	59.8^{+2}_{-2}	$13.2^{+0.3}_{0}$	$2.2^{+0.3}_{0}$	13.3	13.3

Note: units in mm.

12. Land Pattern

Recommended Land Pattern



TOP VIEW

SYMBOL	NOM
A	2.50
B	1.50
C	0.23
D	0.805
E	0.28
F	0.7875
G	0.50
H	1.155
J	1.33

NOTE:
1)LAND PATTERN IS SOLDER MASK DEFINED.
2)IT IS RECOMENDED TO HAVE ON-CU TRACE PCB VIAS.

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.1	2022-09-07	0.1 version setup
0.5	2022-11-25	0.5 version setup
1.0	2022-12-12	1.0 version setup

Important Notice

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