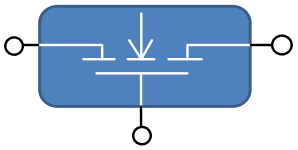
INN040W120A

1. General Description

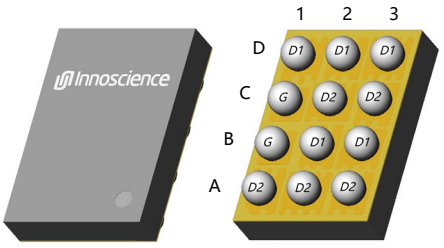
Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in WLCSP with 1.2 mm x 1.7 mm package size.

2. Features



- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance

3. Applications



- High side load switch
- OVP protection in smart phone USB port
- Switch circuits in multiple power suppliers system

4. Key Performance Parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DD,max}$	40	V
$R_{DD(on),max}$ @ V_G = 5 V	12	mΩ
$Q_{G,typ}$ @ V_{DD} = 20 V	7.2	nC
$I_{D,DC}$	10	A

5. Pin Information

Table 2 Pin information

Pin	Pin description	Pin function
D1~3, B2~3	Drain1	Power Drain1
C2~3, A1~3	Drain2	Power Drain2
B1, C1	Gate	Driver Gate

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN040W120A	WLCSP 1.2x1.7	D19

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6. Maximum Ratings

at T_j = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DD}	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	40	V
V_{DG}	Drain-to-Gate Voltage	40	V
V_{GD}	Gate-to-Drain Voltage	6	V
I_D	Continuous Drain current (limited by solder ball)	10	A
I_{DM}	Pulsed Drain Current (25°C, T_{Pulse} = 300 μs)	50	A
T_J	Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-40 to 150	°C

7. Thermal Characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	8.88	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]	67.35	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric Characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{D1D2S}	Drain1-to-Drain2 Breakdown Voltage	40			V	V_{D2} = V_G = 0 V, I_{D1D2} = 500 μA
BV_{D2D1S}	Drain2-to-Drain1 Breakdown Voltage	40			V	V_{D1} = V_G = 0 V, I_{D2D1} = 500 μA
I_{D1D2S}	Zero Gate Voltage Drain Current			20	μA	V_{D2} = V_G = 0 V, V_{D1} = 40 V
I_{D2D1S}	Zero Gate Voltage Drain Current			20	μA	V_{D1} = V_G = 0 V, V_{D2} = 40 V
I_{GDS} (T_J=85°C)	Gate-to-Drain Leakage		0.5	5	μA	V_{D1} = V_{D2} = 0 V, V_G = 5 V
	Gate-to-Drain Leakage	-30			μA	V_{D1} = V_{D2} = 0 V, V_G = -5 V
I_{GDS} (T_J=85°C)	Gate-to-Drain Leakage		5	30	μA	V_{D1} = V_{D2} = 0 V, V_G = 6 V
	Gate-to-Drain Leakage	-40			μA	V_{D1} = V_{D2} = 0 V, V_G = -6 V
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8		2.4	V	V_{D1} = 0 V, V_{D2} = V_G, I_{D2D1} = 1 mA
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8		2.4	V	V_{D2} = 0 V, V_{D1} = V_G, I_{D1D2} = 1 mA
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance		9	12	mΩ	V_{D2} = 0 V, V_{GD} = 5 V, I_{D1D2} = 10 A
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance		9	12	mΩ	V_{D1} = 0 V, V_{GD} = 5 V, I_{D2D1} = 10 A

Table 7 Dynamic characteristics

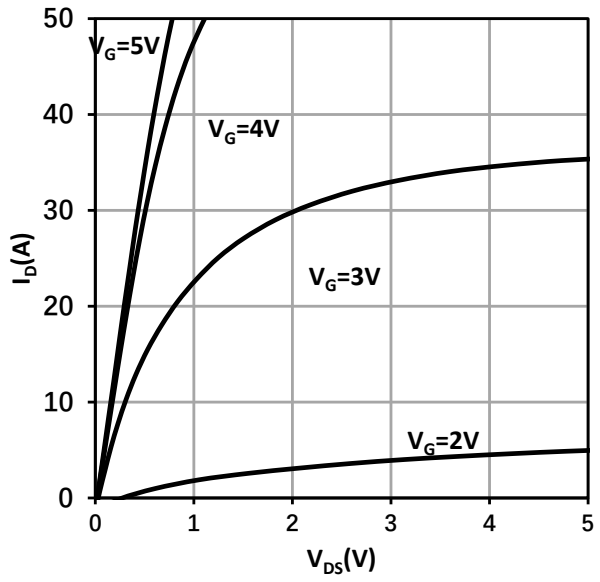
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance		405		pF	V_G = 0 V, V_D = 20 V
C_{OSS}	Output Capacitance		174			
C_{RSS}	Reverse Transfer Capacitance		104			
R_G	Gate Resistance		3.5		Ω	f = 1 MHz
Q_G	Total Gate Charge		7.2		nC	V_D = 20 V, V_G = 5 V, I_D = 10 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D2D1}=20V)		0.9			V_{D1} = 0, V_{D2} = 20 V, I_{D2D1} = 10 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D1D2}=20V)		3.9			V_{D2} = 0, V_{D1} = 20 V, I_{D1D2} = 10 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D1D2}=20V)		0.9			V_{D2} = 0, V_{D1} = 20 V, I_{D1D2} = 10 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D2D1}=20V)		3.9			V_{D1} = 0, V_{D2} = 20 V, I_{D2D1} = 10 A
Q_{OSS}	Output Charge		5.6			V_G = 0 V, V_D = 20 V

9. Electric Characteristics Diagrams

at T_j = 25 °C, unless specified otherwise

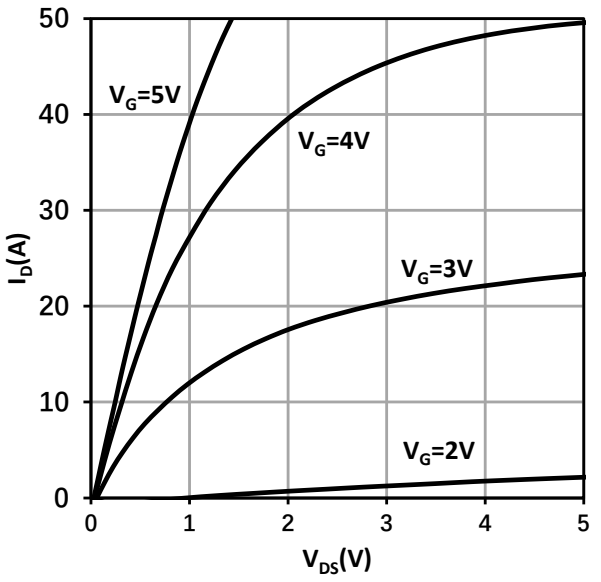
Note: The device characteristics with D1 as drain and D2 as source is the same with D2 as drain and D1 as source.

Figure 1 Typical Output Characteristics



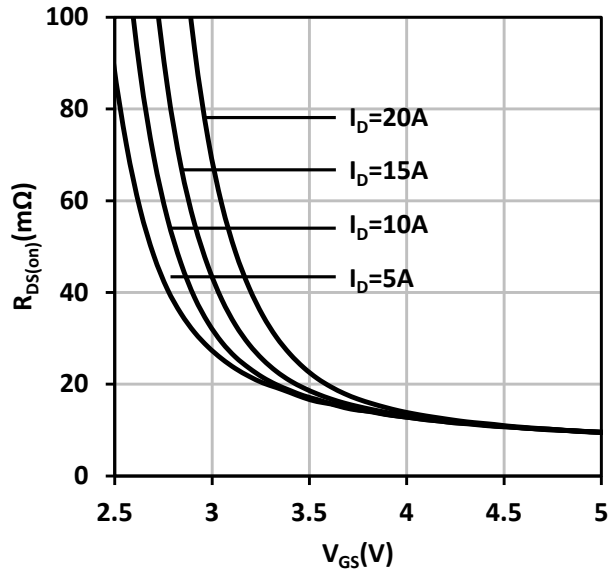
$I_D = f(V_D,V_G)$; T_J = 25 °C

Figure 2 Typical Output Characteristics



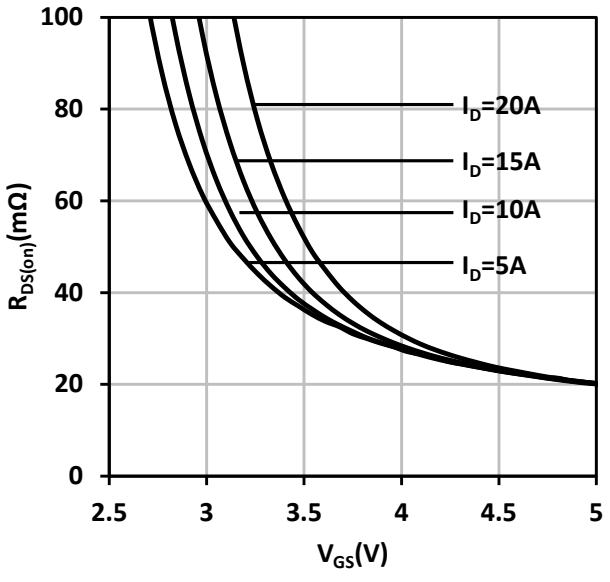
$I_D = f(V_D,V_G)$; T_J = 125 °C

Figure 3 Typical Drain On-state Resistance



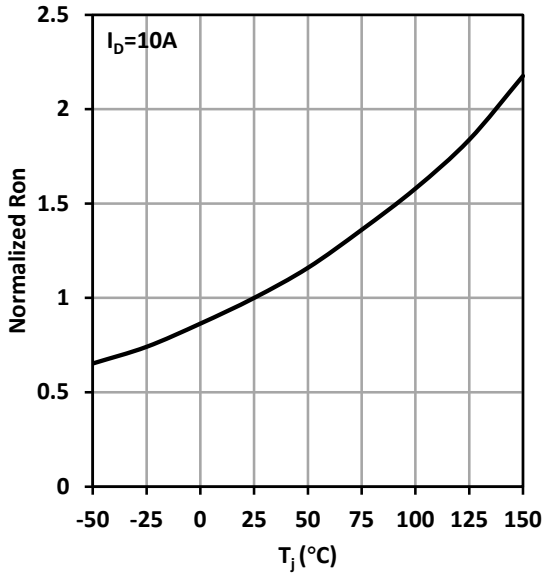
$R_{D(on)} = f(V_G, I_D)$; T_J = 25 °C

Figure 4 Typical Drain On-state Resistance



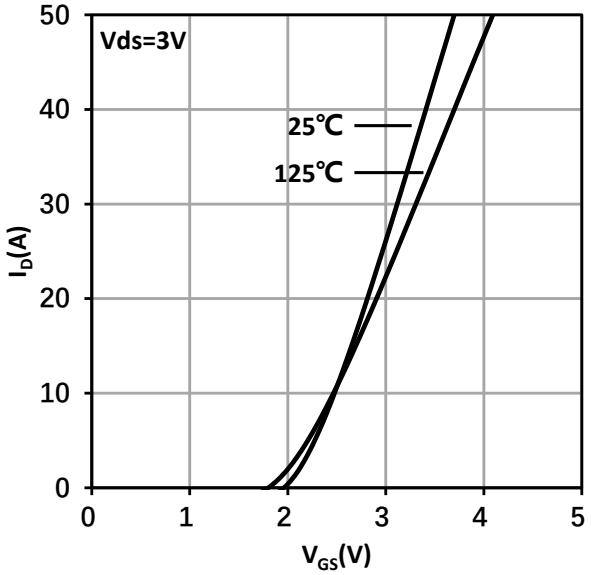
$R_{D(on)} = f(V_G, I_D)$; T_J = 125 °C

Figure 5 Typical On Resistance vs. Temperature



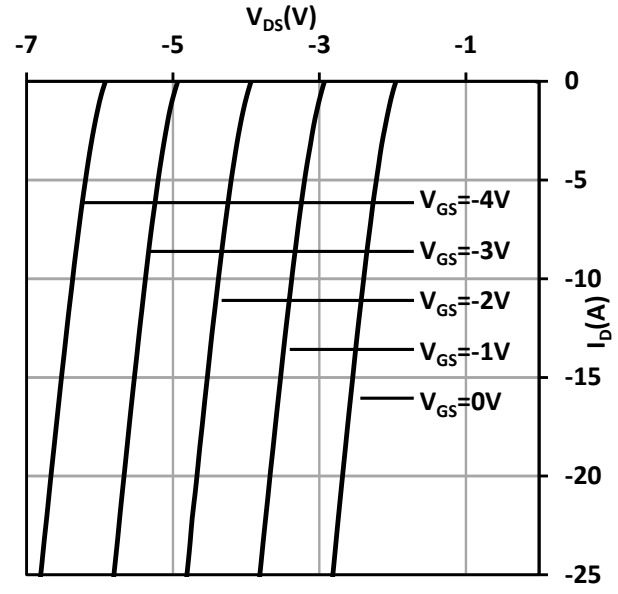
Normalized $R_{D(on)}$ = f(T_J); I_D = 10 A

Figure 6 Typical Transfer Characteristics



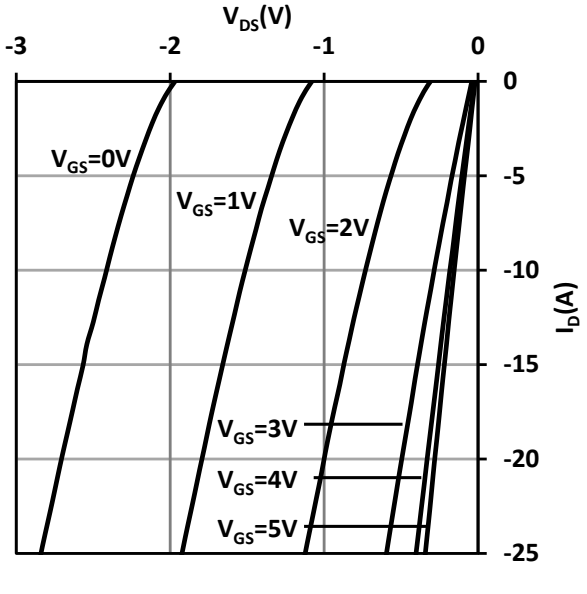
I_D = f(V_G); V_D = 3 V

Fig. 7 Typ. Reverse Drain-Source Characteristics



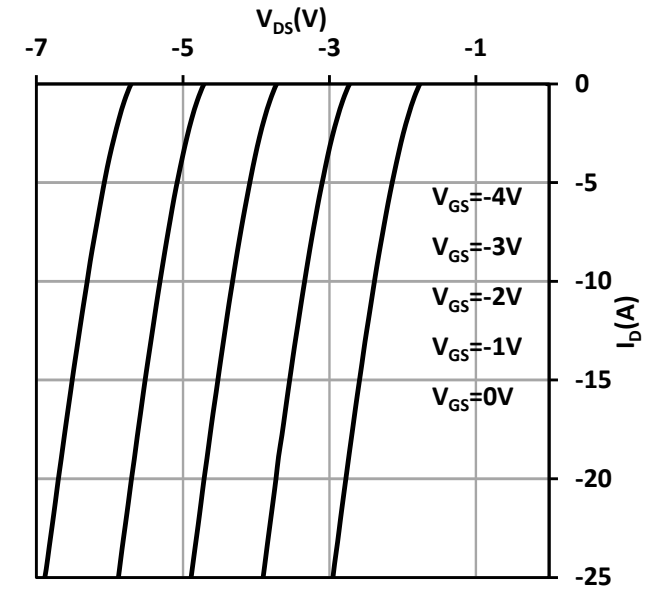
I_D = f(V_D,V_G); T_J = 25 °C

Fig. 8 Typ. Reverse Drain-Source Characteristics



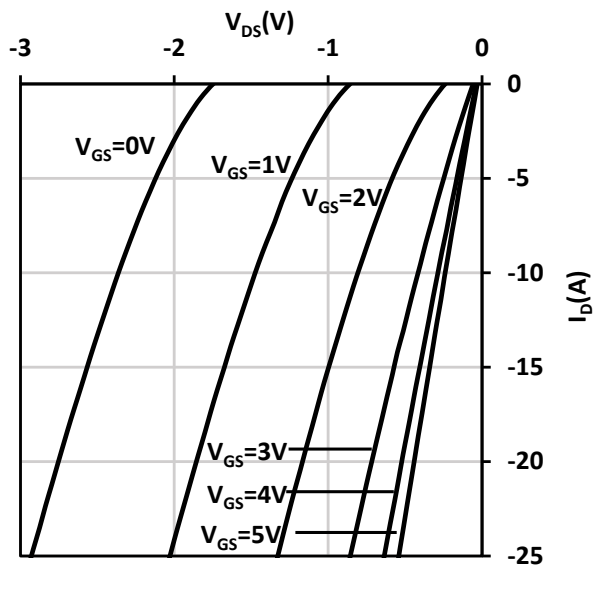
I_D = f(V_D,V_G); T_J = 25 °C

Fig. 9 Typ. Reverse Drain-Source Characteristics



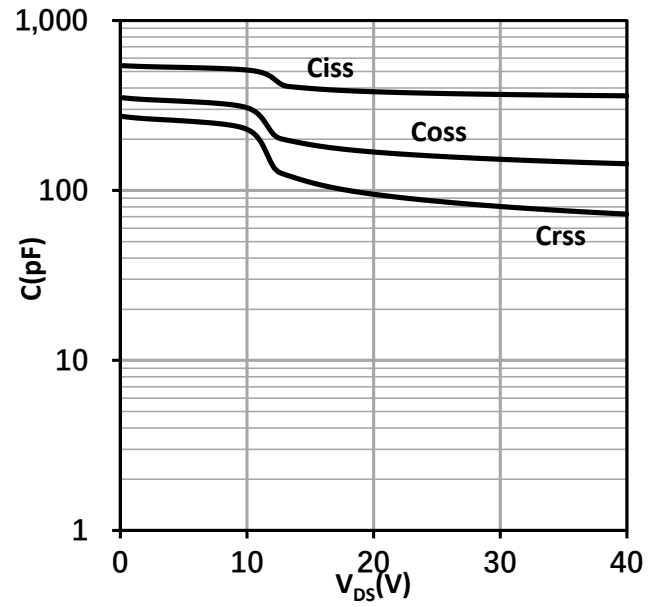
$I_D = f(V_D, V_G)$; T_J = 125 °C

Fig. 10 Typ. Reverse Drain-Source Characteristics



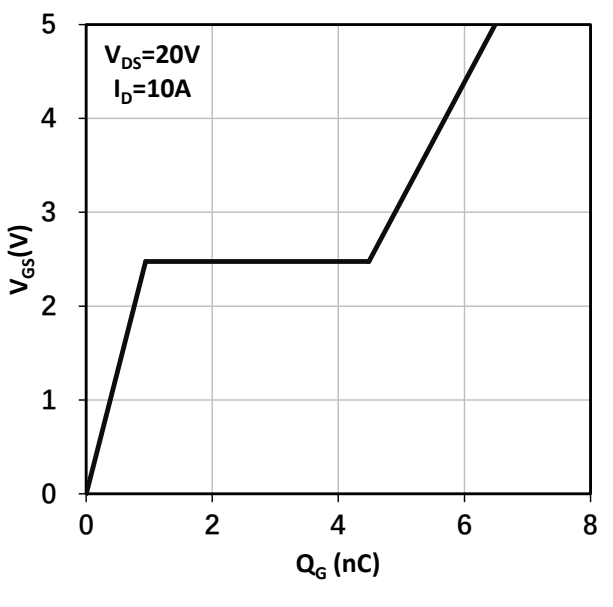
$I_D = f(V_D, V_G)$; T_J = 125 °C

Fig. 11 Typ. Capacitances Characteristics



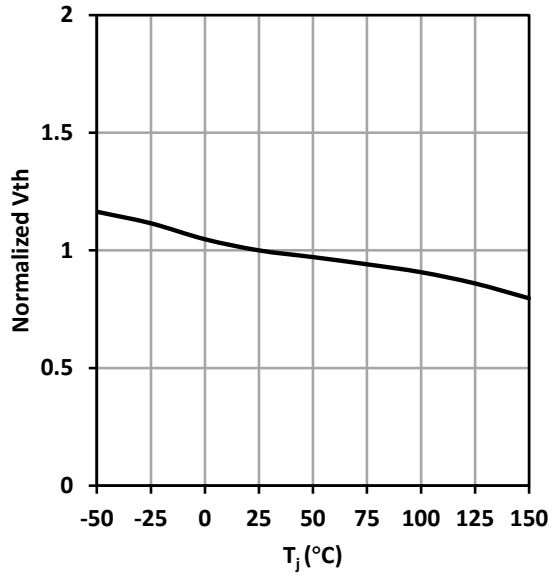
$C_{XSS} = f(V_D)$; f = 1 MHz

Fig. 12 Typ. Gate Charge



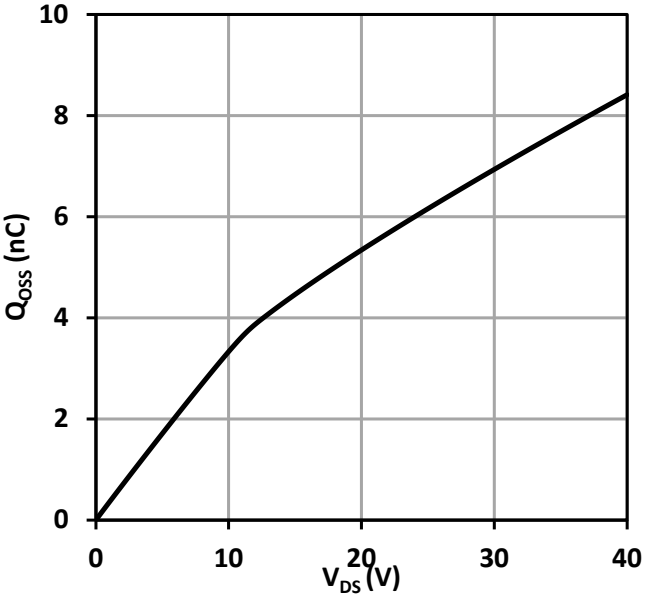
$V_G = f(Q_G)$; V_D = 20 V; I_D = 10 A

Fig. 13 Normalized Threshold Voltage vs. Temp.



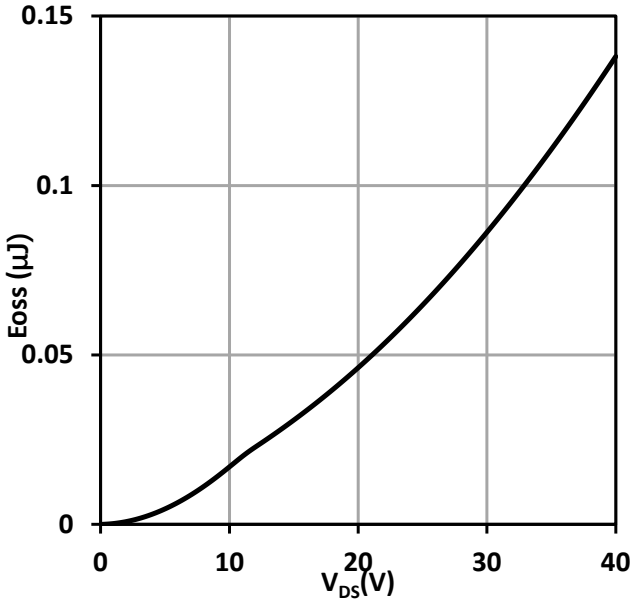
Normalized V_{TH} = f(T_J); V_G = V_D; I_D = 1 mA

Fig. 14 Output Charge



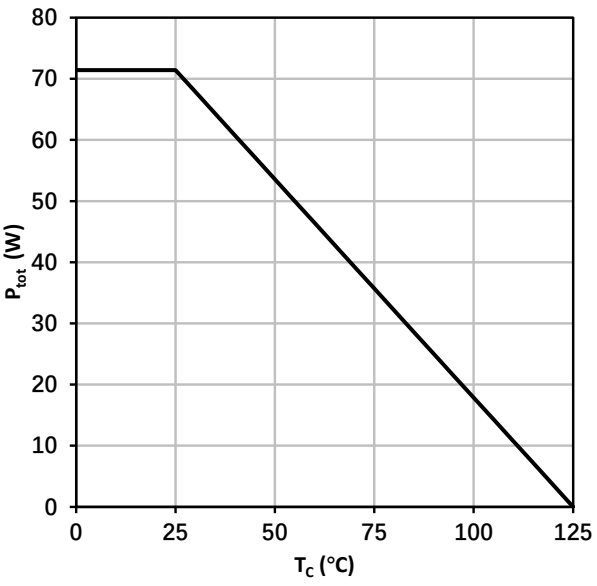
Q_{oss} = f(V_D)

Fig. 15 Output Capacitance Stored Energy



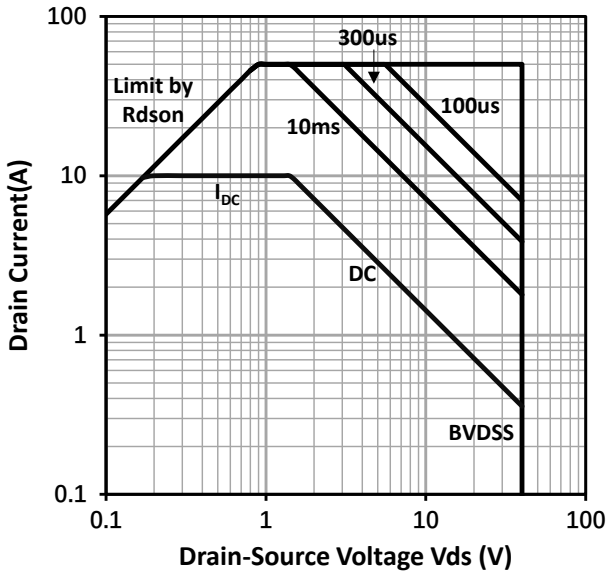
E_{oss} = f(V_D)

Fig. 16 Power Dissipation



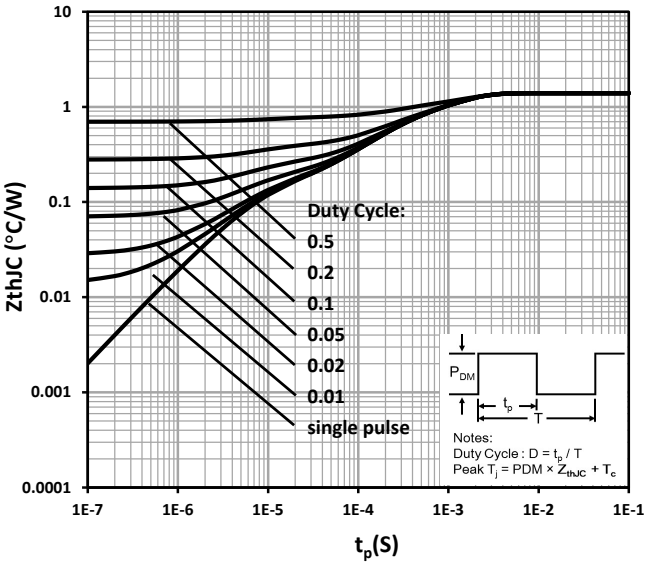
P_{tot} = f(T_B)

Fig. 17 Safe Operating Area



$I_D = f(V_D)$; T_C = 25 ˚C; Single Pulse

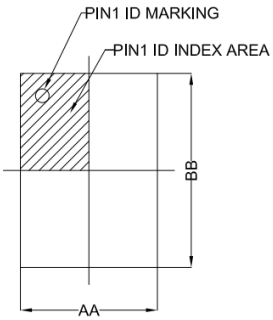
Fig. 18 Max. Transient Thermal Impedance



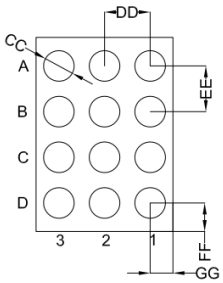
$Z_{\theta JB} = f(t_p)$; parameter: D = t_p / T

10. Package Outlines

Package Reference

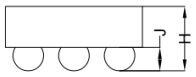


TOP VIEW



BOTTOM VIEW

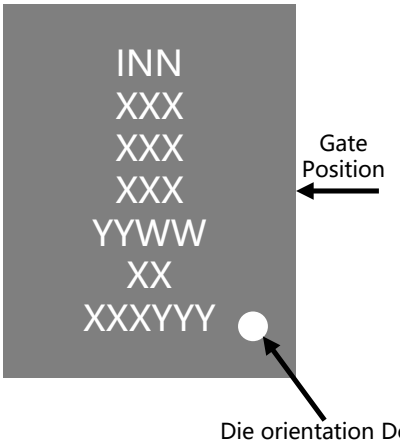
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
AA	1.175	1.200	1.225	
BB	1.675	1.700	1.725	
CC	0.241	0.268	0.295	12X
DD	0.400 BASIC			8X
EE	0.400 BASIC			9X
FF	0.250 REF			4X
GG	0.200 REF			4X
J	0.175	0.205	0.235	
H	0.517	0.564	0.611	



SIDE VIEW

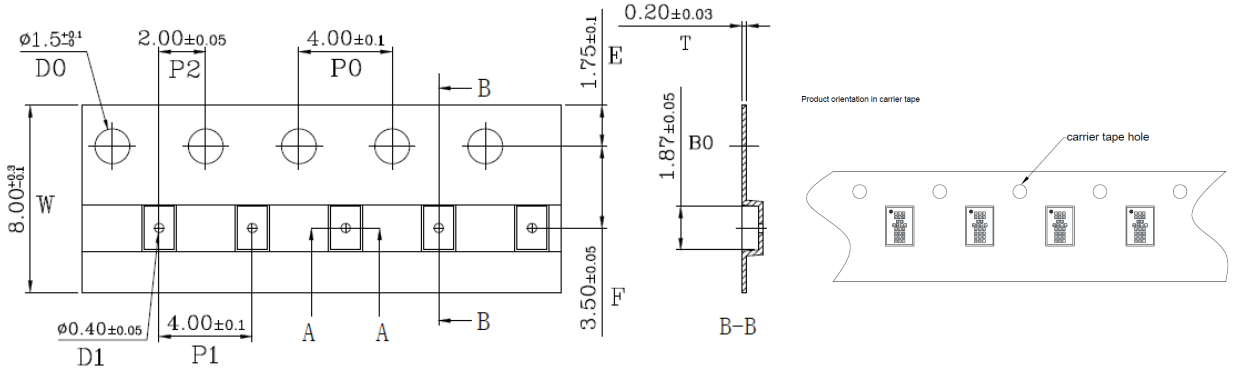
NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS SOLDER BAR VIEW.
3)COMPLIES WITH JEDEC MO-211.
4)DRAWING IS NOT TO SCALE.
5)A,B IS PACKAGE SIZE
6)BAR COPLANARITY SHALL BE 0.05 MILLMETERS MAX

Marking Reference:



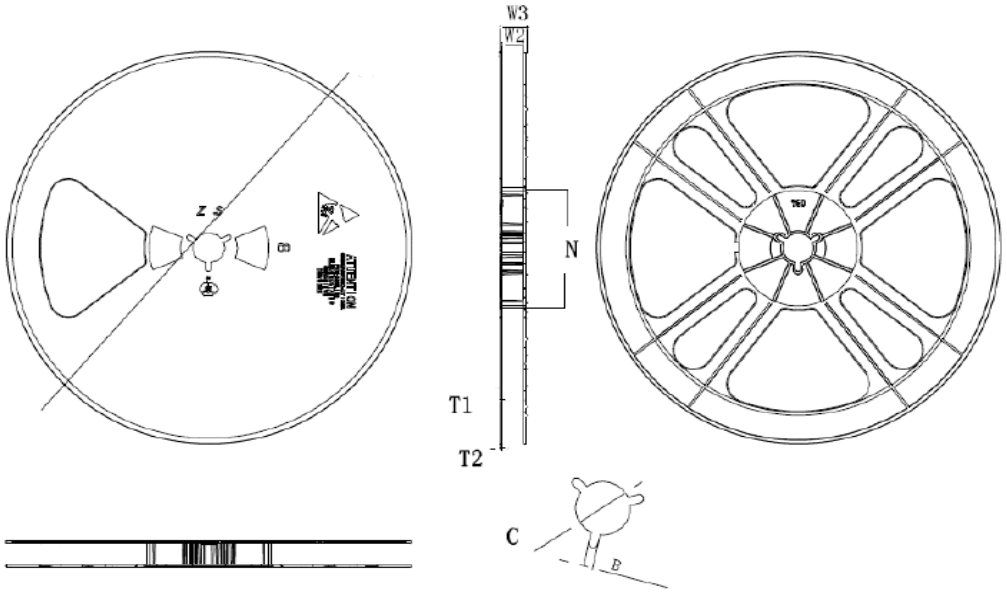
Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Lot code	XXX
Row 4		XXX
Row 5	Date code	YYWW
Row 6	Wafer ID	XX
Row 7	Location ID	XXXYYY

11. Reel Information



Unit: mm

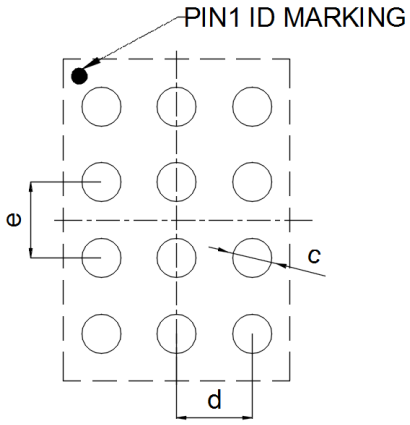
W	P1	E	F	D0	D1	P0	P2	10P0
$8.00^{+0.3}_{-0.1}$	4.00±0.10	1.75±0.10	3.5±0.05	$1.50^{+0.10}_{-0}$	0.4±0.05	4.0±0.1	2±0.05	40±0.2
A0	A1	B0	B1	K0	K1	T		
1.31±0.05		1.87±0.05		0.71±0.05		0.20±0.03		



TYPE	A	N	W2	W3	T1	T2	C	B
8	179±1	54.8±0.2	9.0±0.2	9.2±1.0	1.2±0.2	1.5±0.2	13.5±0.2	2.0±0.2

12. Land Pattern

Recommended Land Pattern



TOP VIEW

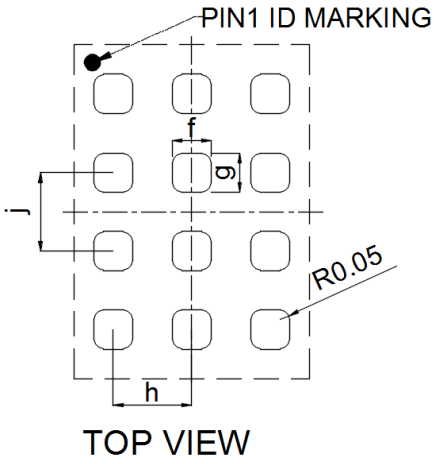
SYMBOL	MILLIMETER	NOTE
	NOM	
c	0.214	12X
d	0.400 BASIC	8X
e	0.400 BASIC	9X

NOTE:

1) LAND PATTERN IS SOLDER MASK DEFINED.

2) IT IS RECOMMENDED TO HAVE ON-CU TRACE PCB VIAS.

Recommended Stencil Drawing



TOP VIEW

SYMBOL	MILLIMETER	NOTE
	NOM	
f	0.200	12X
g	0.200	12X
h	0.400 BASIC	8X
j	0.400 BASIC	9X

13. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-02-10	1.0 version release

Important Notice

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