IS37SML01G8B IS38SML01G8B

IS37SML02G8B IS38SML02G8B

1Gb/2Gb SPI NAND

3.3V 133MHZ MULTI I/O INTERFACE

ADVANCED DATA SHEET

Long-term Support
World Class Quality

1Gb/2Gb 3.3V SPI NAND FLASH MEMORY
104MHz MULTI I/O SPI INTERFACE with Internal ECC

ADVANCED INFORMATION

FEATURES

- **Single-level cell (SLC) technology**

- **Architecture**
  - Memory Cell: 1bit/Memory Cell
  - Page Size: 2176 bytes (2048 + 128) bytes
  - Block Size: 64 pages (128K + 8K) bytes
  - Plane Size:
    1Gb: 1024 blocks per plane
    2Gb: 2048 blocks per plane
  - Device Size:
    1Gb: 1 plane = 1024 blocks
    2Gb: 1 plane = 2048 blocks

- **Standard and extended SPI-compatible serial bus interface**
  - Read: Instruction, address on 1 pin & data out on 1, 2, or 4 pins (1-1-1, 1-1-2 or 1-1-4)
  - Program: Instruction, address on 1 pin; data in on 1, or 4 pins (1-1-1 or 1-1-4)

- **User-selectable Internal ECC**
  - 8 bit ECC per 544 bytes
  - The default state of Internal ECC is enabled.

- **Array performance**
  - Page Read:
    25us (MAX) with Internal ECC disabled
    95us (MAX) with Internal ECC enabled
  - Page Program:
    270us (TYP) with Internal ECC disabled
    320us (TYP) with Internal ECC enabled
  - Erase Block: 4ms (TYP)

- **Operating Voltage Range & Speed**
  - V_{CC} = 2.7V ~3.6V, 133MHz max

- **Operating temperature**
  - Industrial: -40°C to +85°C
  - Automotive, A2: -40°C to +105°C

- **Device Initialization**
  - Automatic device initialization with first page data auto load after power up, with Internal ECC ON always. To use this feature, user needs to write the first page with Internal ECC Enabled.

- **Advanced Commands**
  - Read Read (13h)
  - Read from Cache x1 (03h)
  - Read from Cache x2 (3Bh)
  - Read from Cache x4 (6Bh)
  - Program Load x4 (32h)/Program Load Random Data x4 (34h)
  - Permanent Block Lock Protection (2Ch)

- **Security**
  - **Blocks 7:0 are valid when shipped from factory with Internal ECC enabled.**
  - Software write protection with Block Lock register, which includes BP bits (BP0/1/2)
  - Hardware write protection with WP# to freeze BP bits
  - Lock Tight to protect BP bits during one power cycle instead of WP#
  - Permanent Block Lock protection
  - OTP area: 10 pages one-time programmable (OTP) Flash memory area

- **Reliability**
  - Endurance: Typical 100K Program/Erase cycles with Internal ECC enabled
  - Data Retention: 10 years

- **Industry Standard Pin-out & Packages**
  - J = 8-contact WSON 8x6mm
  - H = 24-ball TFBGA 6x8x1.2 mm
  - Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

GENERAL DESCRIPTION

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non- volatile memory storage solution in systems where pin count must be kept to a minimum.

The ISSI IS37/38SML01G8B/02G8B are 1Gb/2Gb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation.

1Gb is organized as 1024 blocks for 1Gb. 1 plane for 1Gb, 64 pages per block, 2176 bytes per page (2048 + 128 bytes).

2Gb is organized as 2048 blocks for 2Gb. 1 plane for 2Gb, 64 pages per block, 2176 bytes per page (2048 + 128 bytes).

When internal ECC is enabled, only 64 spare bytes could be accessed by user (User accessible page size = 2048 + 64 = 2112 bytes). The other 64 spare bytes used as ECC parity bytes internally.

The block size is 28KB + 8KB. The device has a cache register of 2176 bytes length, which allows data to be transferred between the cache and the cell array during page read and page program operation. The erase operation is implemented in unit of block.

The device provides the advanced write protection mechanism for the data security, like software write protection with block lock register, which includes BP1, BP1, and BP2 bits. Also hardware write protection with WP# and permanent block lock protection command are supported.

New features include user-selectable Internal 8-bit ECC and first page auto-load on power up. With internal ECC enabled as the default after power on, ECC code is generated internally when a page is written to memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary.

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The Internal ECC can be disabled or enabled again by command. When the Internal 8-bit ECC logic is disabled, the host must handle the 8-bit ECC.

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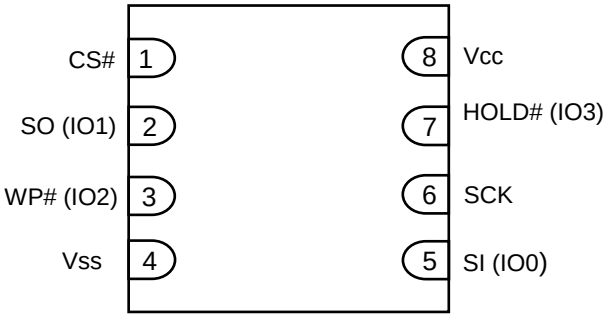
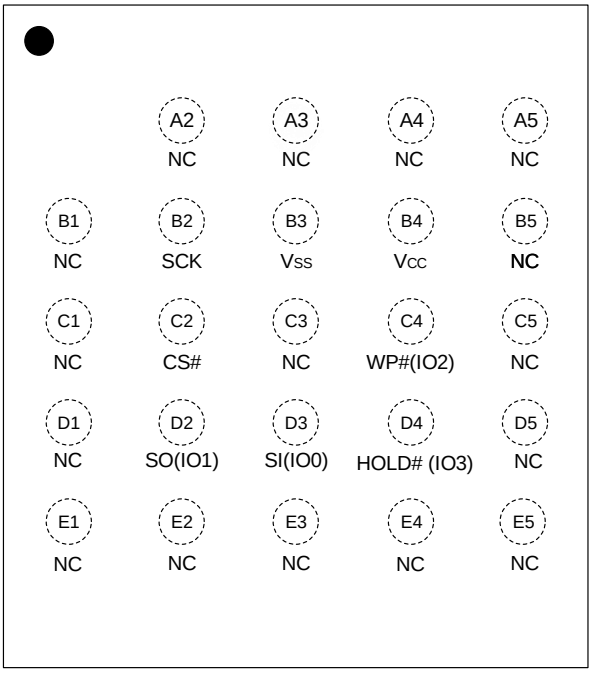
1. PIN CONFIGURATION AND DESCRIPTION

8-contact WSON 8x6mm



24-ball 5x5 ball array TFBGA

Top View, Balls Facing Down



Symbol	Type	Pin Function
CS#	Input	**Chip Select:** The device selection control.
SCK	Input	**Serial Clock:** The serial clock input.
WP#	Input	**Write Protect:** When LOW, prevents overwriting block lock bits (x1/x2 operation).
HOLD#	Input	**Hold:** Hold function is disabled by default. When enabled, the external pull-up register is necessary to avoid accidental operation being placed on hold. Hold# pauses any serial communication with the device without deselecting it (x1/x2 operation).
SI/IO0, SO/IO1, IO2, IO3	I/O	**Serial I/O:** The bidirectional I/O signals transfer address, data, and command information. SI and SO for x1 operation, I/O0 and I/O1 for x2/x4 operations, and I/O2 and I/O3 for x4 operation.
V_{CC}		**POWER:** V_{CC} is the power supply for device.
V_{SS}		**GROUND**

2. BLOCK DIAGRAM

The devices use an industry standard NAND Flash memory core organized by page/block with SPI interface.

The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. The modifications are specially to handle functions related to NAND Flash architecture. The interface supports page and random read/write and internal data move functions. The device also includes an Internal ECC feature.
Data is transferred to or from the cell array, page-by-page, to a cache register and a data register. The cache register is closest to the I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations; it is erased in block-based operations. The cache register functions as the buffer memory to enable random data READ/WRITE operations. These devices also use a new SPI status register that reports the status of device operation.

Figure 2.1 Functional Block Diagram

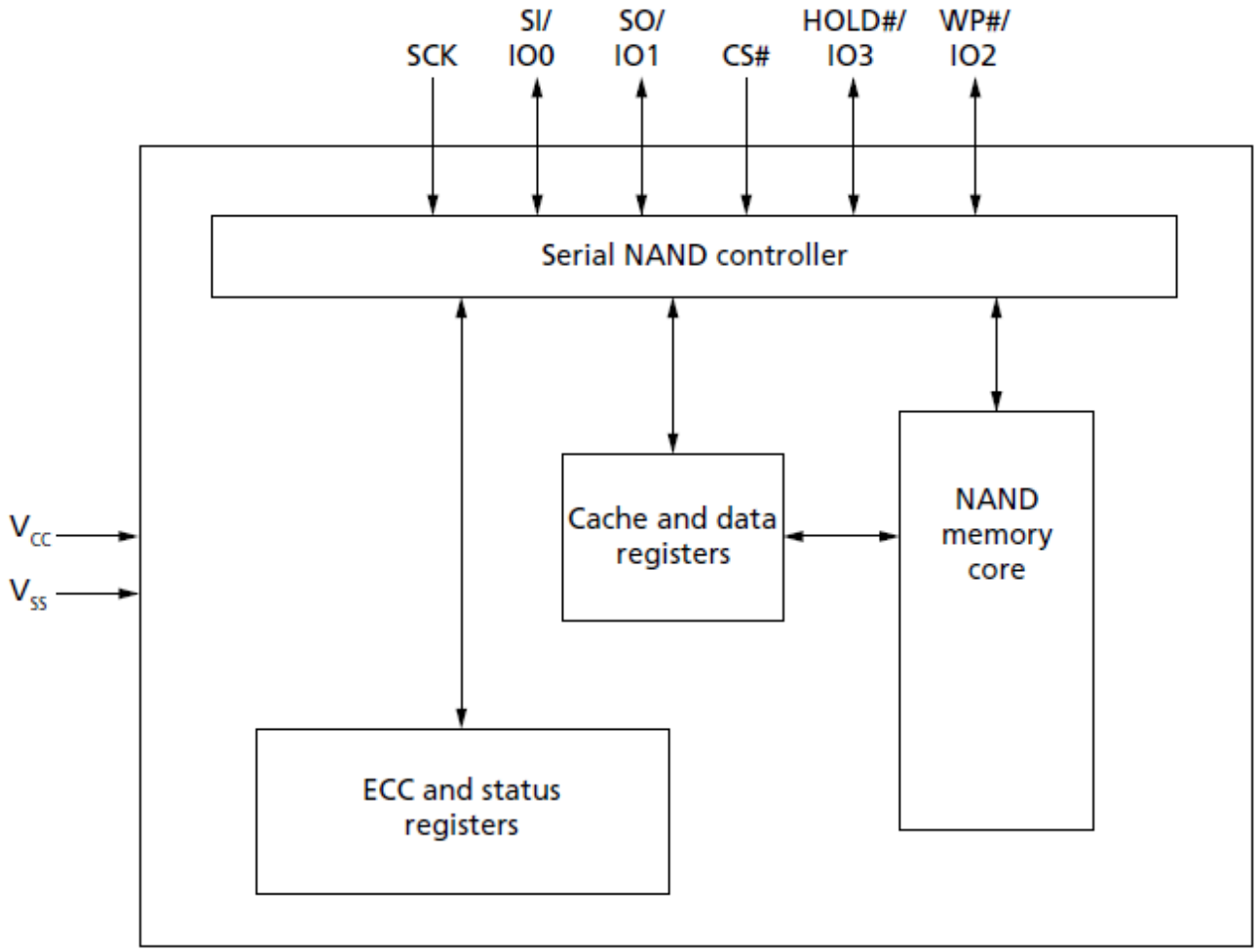
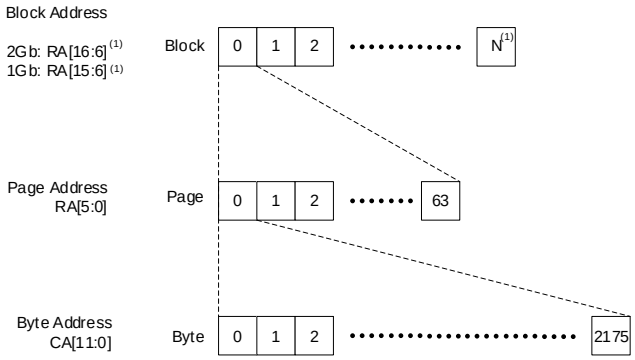


Figure 2.2 Memory Map



Note:
1. N = 1023 for 1Gb, 2047 for 2Gb.

3. FEATURE OPERATIONS AND REGISTERS

3.1 GET FEATURE (0FH) AND SET FEATURE (1FH)

The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands either monitor the device status or alter the device configuration from the default at power-on. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP protect, block locking can be managed by setting specific bits in feature address A0h and B0h. Typically, the status register at feature address C0h is read to check the device status, except WEL, which is writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to by SET FEATURE command. Unless specified otherwise, once the device is set, it remains set even if a RESET (FFh) command is issued. CFG [2:0] will be cleared to 000 after a reset and the device is back to normal operation.

Notes:
1. SET FEATURE command only could be executed during device is ready state (OIP = 0); otherwise tis command would be ignored.

Figure 3.1 GET FEATURE (0Fh) Timing

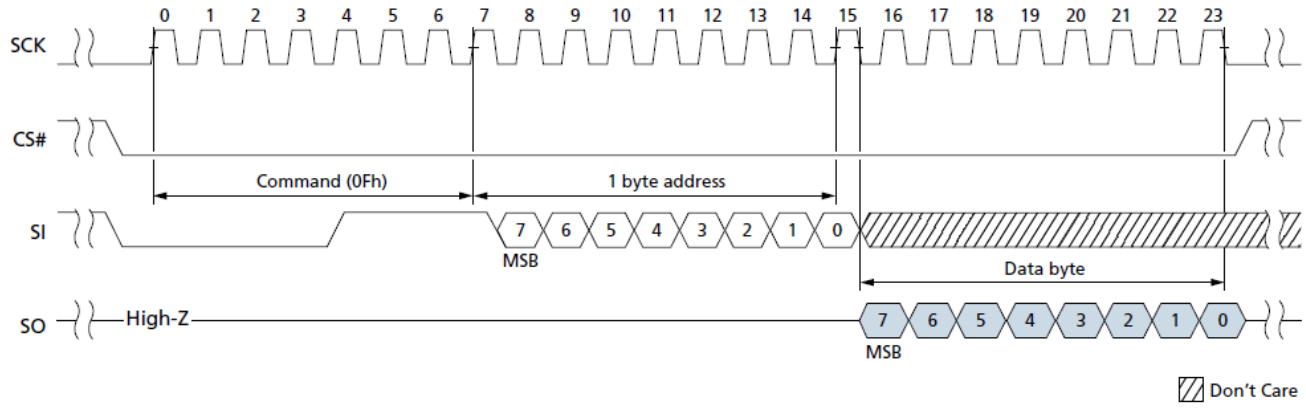
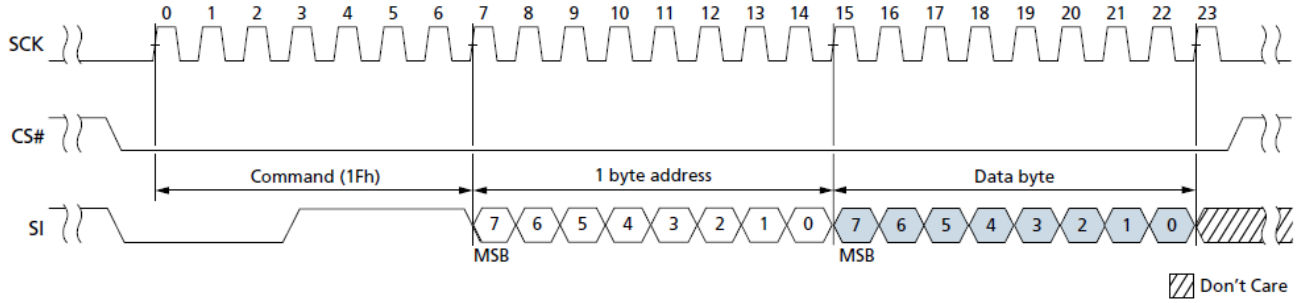


Figure 3.2 SET FEATURE (1Fh) Timing



3.2 FEATURE SETTINGS

Table 3.1 Feature Address Settings and Data Bits

Register	Feature Address	Feature Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	Address = A0h; Access = R/W	BRWD (1)	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Configuration	Address = B0h; Access = R/W	OTP CFG2	OTP CFG1	LOT_Enable	ECC_Enable	Reserved	Reserved	OTP CFG0	QE
Status	Address = C0h; Access = R	Reserved	ECCS2	ECCS1	ECCS0	P_Fail	E_Fail	WEL	OIP
Drive strength	Address = D0h; Access = R/W	Reserved	DRS1	DRS0	Reserved	Reserved	Reserved	Reserved	Reserved

Note:
1. If BRWD (block lock register write disabled) is enabled and WP# is LOW, then bits 7, 5, 4, 3, 2, and 1 at the Block Lock register cannot be changed.

3.3 BLOCK LOCK REGISTER

This register contains volatile block protection bits and BRWD bit. The default value of this register is 3Eh after power-up.

Table 3.2 Block Lock Register

Bit	Name	Attribute	Description
7	BRWD	R/W	Default = 0; when BRWD = 1, enable hardware protection mode with WP# = low
6	Reserved	R only	Default = 0
5	BP2	R/W	Default = 111XX to protect entire array
4	BP1	R/W	
3	BP0	R/W	
2	INV	R/W	
1	CMP	R/W	
0	Reserved	R only	Default = 0

3.4 CONFIGURATION REGISTER

Table 3.3 Configuration Register

Bit	Name	Attribute	Description
7	OTP_CFG2	R/W	Default = '000' to enable normal operation '010' to enable OTP access '110' to enable OTP data protection bit access '111' to enable Boot block lock protection configuration bit access Others to enable normal operation
6	OTP_CFG1	R only	
1	OTP_CFG0	R/W	
5	LOT_Enable	R/W	BP bits, INV, CMP and BRWD bit Protection bit. Default = 0 indicates no protection after device initialization.
4	ECC_Enable	R/W	Internal ECC ON/OFF bit; Default = 1 indicates internal ECC is enabled after device initialization.
3	Reserved	R only	Default = 0
2	Reserved	R only	Default = 0
0	QE	R/W	Quad mode enable/disable bit; Default = 0 indicates Quad mode is disabled.

OTP Configuration Bits (OTP_CFG2, 1, 0)
10 pages OTP area of 2176 or 2112-byte are provided to store critical data that cannot be changed once OTP DATA protection bit is set to '0'.

To protect boot block lock protection from further change, the device also provides a nonvolatile configuration to disable boot block lock protection for the user. This is also implemented the program Execute by reserving one page of Flash array to store this configuration bit.

OTP_CFG2,1,0 controls the access entry to above different operations. The default value after power up or a RESET command is 0.

Lock Tight Enable Bit (LOT_Enable)
10 pages OTP area of 2176 or 2112-byte are provided to store critical data that cannot be changed once OTP DATA protection bit is set to '0'. LOT_Enable bit provides a software protection to protect BP bits, INV, CMP, and BRWD bit when hardware protection mode is disabled by Quad operation.

Note that once this bit is set to '1', only power-down and power up cycle could change this bit to '0' state.

ECC_Enable Bit (ECC_Enable)
The device has an internal ECC algorithm that can be used to obtain the data integrity. Internal ECC calculation is done during page programming, and the result is stored in reserved ECC area for each page. During array read operation, ECC engine will verify the data value according to stored ECC information and to make necessary corrections if needed. Correction status is indicated by the ECC status bits.
ECC_Enable = 1 indicates internal ECC turned-on; ECC_Enable = 0 indicates internal ECC turned-off.
ECC_Enable will be '1' after device initialization (default=1).

Quad Enable Bit
QE bit is designed to support x4 mode and enable x4 mode commands. During x4 mode, WP#/OLD# is used as IIO2/IO3 respectively. The user might not drive these two pins during command or address cycles; this might cause some accidental hardware protection mode enabled or accidental HOLD condition entry in applications.

This bit could be used to disable hardware protection mode and HOLD condition as well as enable x4 command acceptance.

3.5 STATUS REGISTER

Status register bits show the device status.
The status register bits can be read out during the device operation. All bits are read-only register except WEL, which could be changed by WRITE DISABLE (04h) and WRITE ENABLE (06h) commands. None of bits can be changed by SET FEATURE command (1Fh).
The status register can be read by issuing the GET FEATURE (0Fh) command, followed by the feature address (C0h). The status register will output the status of the operation.

Table 3.4 Status Register

Bit	Name	Description
7	Reserved	
6	ECCS2	ECC status provides ECC status as follows; 000b = No bit errors detected during the previous read algorithm. 0001b = 1 to 3 bit errors detected and corrected; no data refreshment is required. 010b = More than 8 bit errors detected and not corrected. 011b = 4 to 6 bit errors detected and corrected; data refreshment is recommended. 100b = Reserved. 101b = 7 to 8 bit errors detected and corrected; data refreshment is mandatory. 110b = reserved. 111b = Invalid state. ECC status is set to 000b either following a RESET or at the beginning of PAGE READ. It is then updated after the device completes a valid READ operation. ECC status is invalid if ECC is disabled (via a SET FEATURE command to B0h address). After a power-up RESET or device initialization, ECC status is set to reflect the contents of block 0, page 0.
5	ECCS1	
4	ECCS0	
3	Program fail (P_Fail)	Indicates that a program failure has occurred (P_FAIL = 1). This bit will also be set if the user attempts to program an invalid address or a locked or protected region, including the OTP area. This bit is cleared (P_FAIL = 0) during the PROGRAM EXECUTE command sequence or a RESET command.
2	Erase fail (E_Fail)	Indicates that an erase failure has occurred (E_FAIL = 1). This bit will also be set if the user attempts to erase a locked region or if the ERASE operation fails. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or a RESET command.
1	Write Enable Latch (WEL)	Indicates the current status of the write enable latch (WEL) and must be set to 1 prior to issuing a PROGRAM EXECUTE or BLOCK ERASE. This bit will be set (WEL=1) by issuing WRITE ENABLE command. This bit is cleared (WEL=0) by issuing WRITE DISABLE command or successful program/erase operation.
0	Operation In Progress (OIP)	This bit is set to 1 when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, PROTECTION or RESET command is executing, or a power-up initialization is executing; the device is busy. When the bit is 0, the interface is in the ready state.

3.6 DRIVE STRENGTH REGISTER

The Drive Strength bits can be used to adjust output pin drive strength. Default value for Drive Strength is 50 % (DRS1 = 1, DRS0 = 0).

Table 3.5 Drive Strength Bits

DRS1	DRS0	Attribute
0	0	100%
0	1	75%
1	**0**	**50% (default)**
1	1	25%

4. BUS OPERATION AND COMMAND DESCRIPTION

4.1 SPI MODE

The device can be driven by a host with its SPI running in either of two modes depending on clock polarity (CPOL) and clock phase (CPHA) settings:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

The difference between two modes is that the clock polarity when the bus master is in standby mode and not transferring data.

- **SCK =0 for CPOL = 0, CPHA = 0 (Mode 0)**
- SCK =1 for CPOL = 1, CPHA = 1 (Mode 3)

4.2 SPI NAND COMMAND DEFINITIONS

Table 4.1 Command Set

Command	Op Code	Add. Bytes	Dummy Bytes	Data Bytes	Comments
Reset Operations					
RESET	FFh	0	0	0	Reset the device
Identification Operation					
READ ID	9Fh	0	1	2	Read Device ID
Feature Operation					
GET FEATURE	0Fh	1	0	1	Get feature
SET FEATURE	1Fh	1	0	1	Set feature
Read Operation					
PAGE READ	13h	3	0	0	Array read
READ from CACHE x1	03h, 0Bh	2	1	1 to 2176(1)	Output cache data at column address
READ from CACHE x2	3Bh	2	1	1 to 2176(1)	Output cache data on IO[1:0]
READ from CACHE x4	6Bh	2	1	1 to 2176(1)	Output cache data on IO[3:0]
Write Enable/Disable Operation					
WRITE ENABLE	06h	0	0	0	Set the WEL bit in the status register to 1
WRITE DISABLE	04h	0	0	0	Clear the WEL bit in the status register to 0
Erase Operation					
BLOCK ERASE	D8h	3	0	0	Block Erase
Program Operation					
PROGRAM EXECUTE	10h	3	0	0	Array program
PROGRAM LOAD x1	02h	2	0	1 to 2176(1)	Load program data into cache register on SI
PROGRAM LOAD x4	32h	2	0	1 to 2176(1)	Load program data into cache register on IO[3:0]
PROGRAM LOAD RANDOM DATA x1	84h	2	0	1 to 2176(1)	Overwrite cache register with input data on SI
PROGRAM LOAD RANDOM DATA x4	34h	2	0	1 to 2176(1)	Overwrite cache register with input data on IO [3:0]
PERMANENT BLOCK LOCK PROTECTION	2Ch	3	0	0	Permanently protect a specific group of blocks

Note:

1. **Depending on Internal ECC ON or OFF; byte 0 to 2175 are valid for user access when Internal ECC OFF; byte 0 to 2111 are valid for user access when Internal ECC ON.**

In this product, every instruction sequence starts with one-byte instruction code. Depending on instruction, the instruction sequence involves shifting in address bytes and/or data bytes. Some instruction donot have any address or data bytes.

In the case of Read (Get Feature, all types of read from cache, Read ID) instructions, the shifted-in instruction sequence is followed by a data-out sequence. CS# can be driven HIGH at any time during data-out sequence.

In the case of write instructions (Block Erase, Program Execute, all types of Program Load, Write Enable, Write Disable, Permanent block Lock protection, Set Feature), Page Read (13h) and Reset (FFh) instructions, CS# must be driven HIGH after whole instruction sequence is completed. Otherwise, the instruction is not executed and the state of WEL remains unchanged if these instructions that alter the array or device configuration require Write Enable Latch (WEL) bit to be set.

4.3 SERIAL INPUT AND OUTPUT TIMING

Figure 4.1 Serial Input Timing

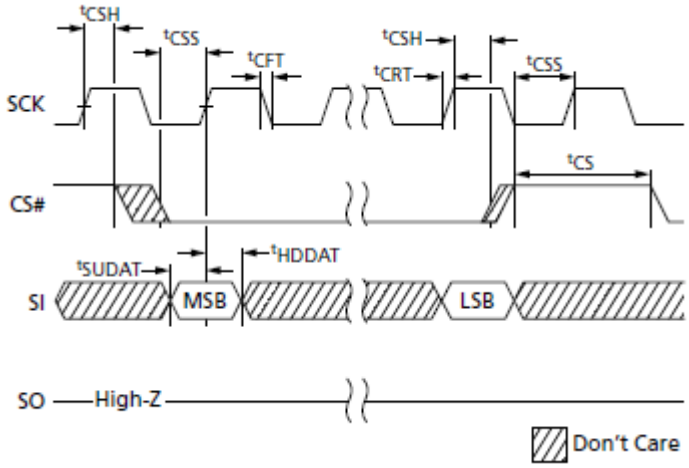


Figure 4.2 Serial Output Timing

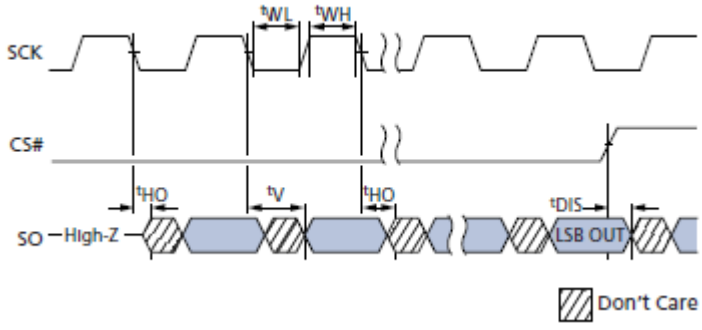


Figure 4.3 WP# Timing

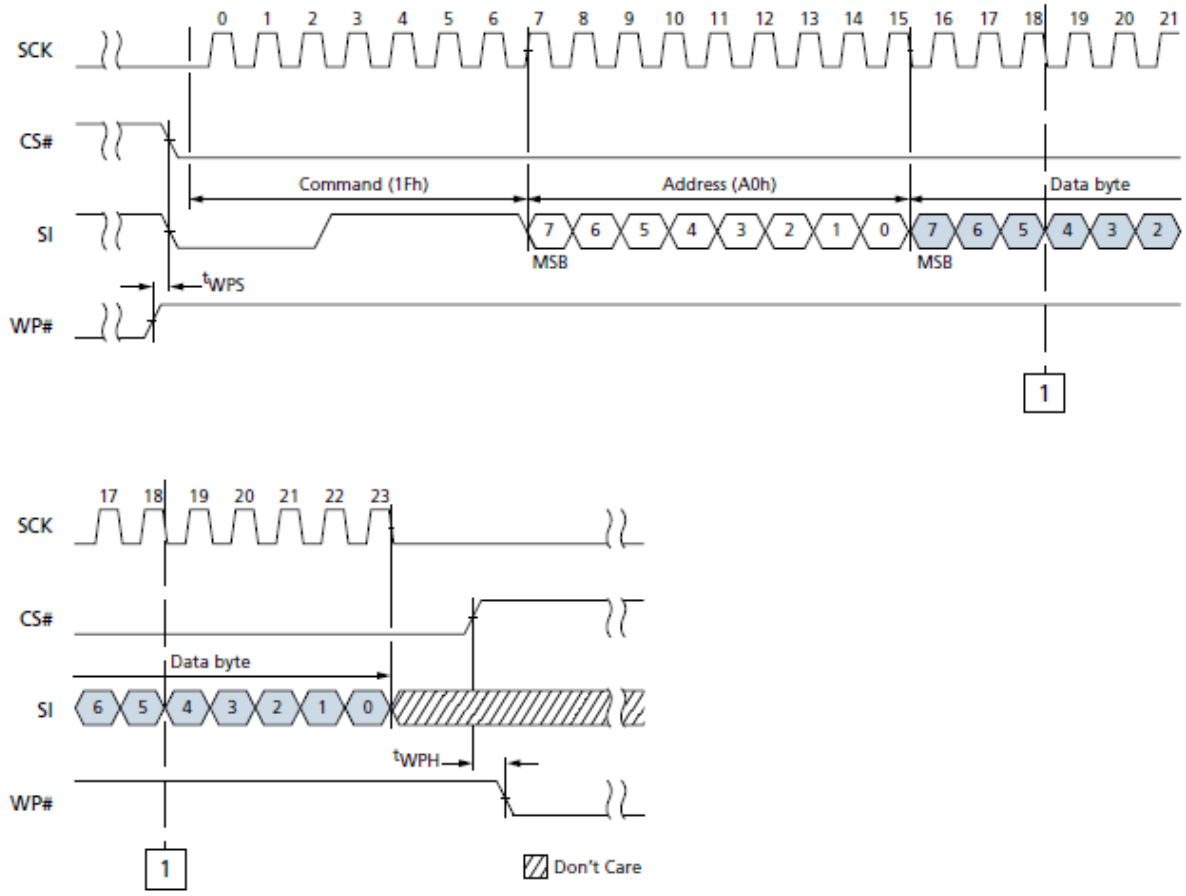
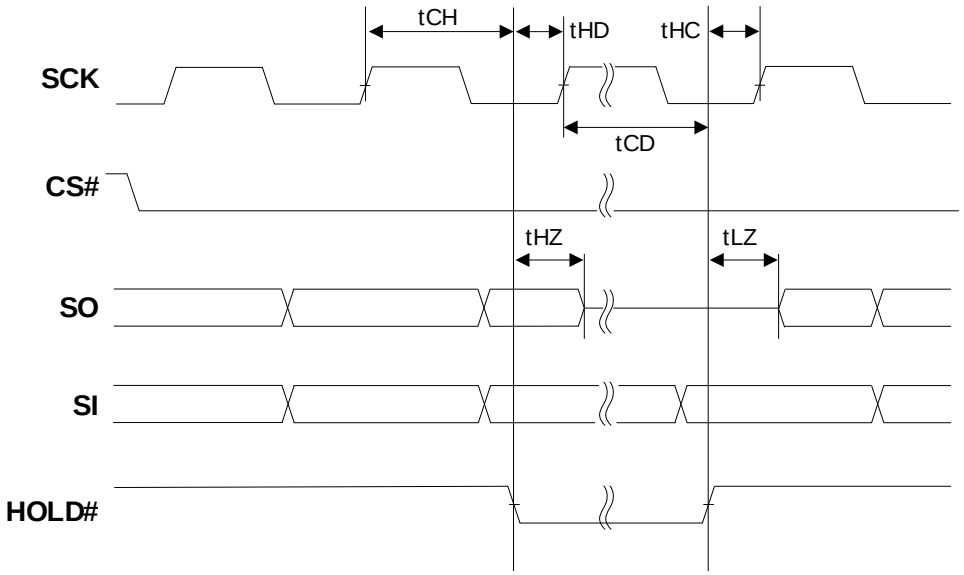


Figure 4.4 HOLD# Timing



5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature (T_{STG})		-65°C to +150°C
Supply Voltage (V_{CC})	3.3V device	-0.6V to +4.6V
Voltage Applied to Any Pin (V_{IN})	3.3V device	-0.6V to +4.6V

Notes:
1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

5.2 RECOMMENDED OPERATING CONDITIONS

Operating Temperature	Industrial Grade	-40°C to 85°C
	Automotive Grade A1	-40°C to 105°C
V_{CC} Supply Voltage	3.3V device	2.7V (VMIN) – 3.6V (VMAX); 3.3V (Typ)

5.3 AC PIN CAPACITANCE (TA = 25°C, VCC= 3.3V, 54MHZ)

Symbol	Parameter	Test Condition	Min	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	-	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	-	8	pF

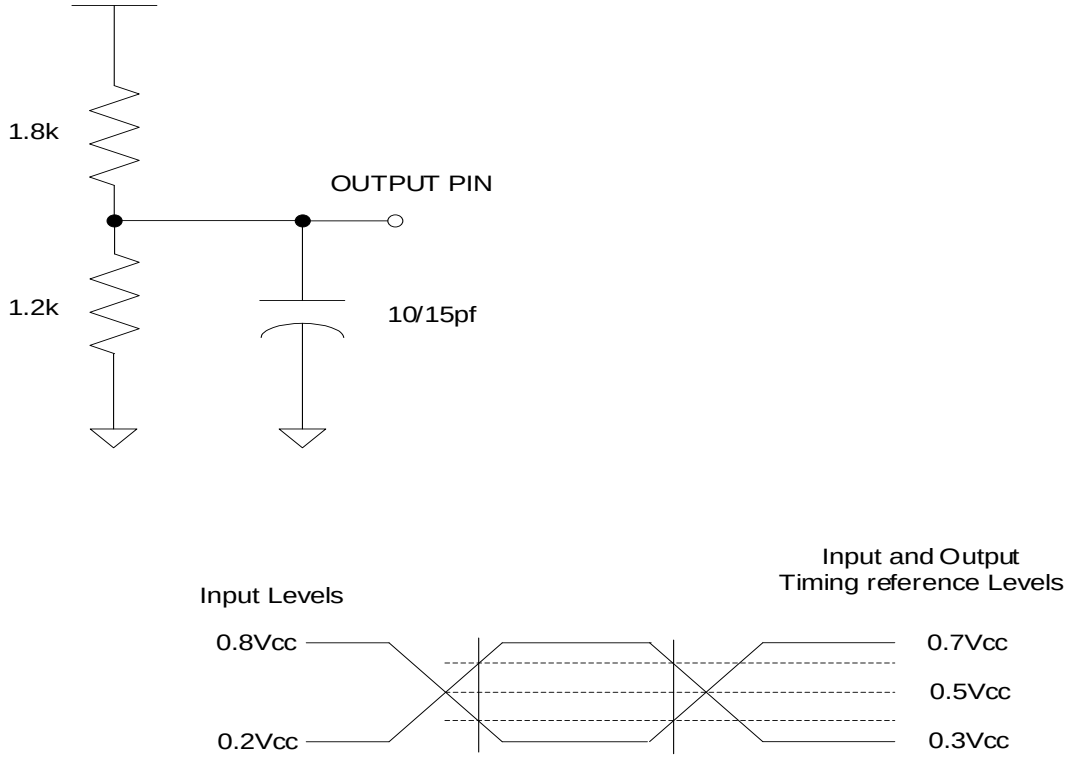
Note:
1. These parameters are characterized and not 100% tested.

5.4 AC MEASUREMENT CONDITION

Symbol	Parameter	Min	Max	Units
CL	Output Load	1 TTL GATE and CL = 15/10		pF
TR, TF	Input Rise and Fall Times (1)		5	ns
	Input Rise and Fall Times (80MHz or faster) (2)		2.1	
	Input Rise and Fall Times (100MHz or faster) (2)		1.5	
VREFI	Input Timing Reference Voltages	$0.3V_{CC}$	$0.7V_{CC}$	
VREFO	Output Timing Reference Voltages	$0.5V_{CC}$		

Notes:
1. Applicable to 20MHz or 66MHz.
2. 20% of clock period.

Figure 5.1 Output test load & AC measurement I/O Waveform



Note:
1. For Dual and Quad operations rail-to rail assumed for input levels.

5.5 DC CHARACTERISTICS

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit	Notes
	Stand-by Current (CMOS)	ICC1(2)	CS#=V_{CC}, V_{IN}=V_{SS} or V_{CC}	-	10	50	uA	
Operating Current	Sequential Read (x1)		SCK = 0.1V_{CC}/0.9V_{CC} 133MHz, SO=open	-	-	16	mA	
	Sequential Read (x2)		SCK = 0.1V_{CC}/0.9V_{CC} 133MHz	-	-	20		
	Sequential Read (x4)		SCK = 0.1V_{CC}/0.9V_{CC} 133MHz	-	-	22		
	Page Read	ICC3(4)	CS#=V_{CC}	-	7.5	15		
	Program	ICC4(5)	CS#=V_{CC}	-	7.5	15		
	Erase	ICC5	CS#=V_{CC}	-	7.5	15		
Power-Up current		ICC6 (6)		-	-	10	mA	
Input Leakage Current		I_{LI}	V_{IN} = 0V to V_{CC}	-	-	+/-10	uA	
Output Leakage Current		I_{LO}	V_{OUT} = 0V to V_{CC}	-	-	+/-10	uA	
Input High Voltage		V_{IH} (3)	-	0.7xV_{CC}	-	Vcc+0.4	V	
Input Low Voltage, All inputs		V_{IL} (3)	-	-0.5	-	0.3xV_{CC}		
Output High Voltage Level		V_{OH}	I_{OH} = -100 uA	V_{CC}-0.2	-	-		
Output Low Voltage Level		V_{OL}	I_{OL} = 1.6 mA	-	-	0.4		

Notes:

1. All currents are RMS unless noted. Typical values at typical V_{CC} (3.3V), V_{IO} = 0V/V_{CC}, T_C = 25°C.
2. Standby current is the average current measured over any 5ms time interval 5us after CS# deassertion (and any interval operations are completed).
3. All read currents are average current measured over any 2KB continuous reads. No Load, checker board pattern.
4. All page read currents are average current measured over any one page read checker board pattern.
5. All program currents are average current measured over any 2KB typical data program.
6. Measurement is taken over 1.25ms with interval 5us and begins after V_{CC} reaches V_{CC} min.
7. VIL can undershoot to -1.0V for periods <2ns and VIH can overshoot to V_{CC} (max)+1V for periods <2ns.

5.6 AC CHARACTERISTICS FOR ADDRESS/ COMMAND/DATA INPUT

Parameter		Symbol	Alt.	Min	Max	Unit
Clock frequency		fC	fC	-	133	MHz
Clock LOW time		tCL(2)	tWL	3.375	-	ns
Clock HIGH time		tCH(2)	tWH	3.375	-	ns
Clock rise time		tCLCH(3)	tCRT	1.3	-	V/ns
Clock fall time		tCHCL(3)	tCFT	1.3	-	V/ns
Command deselect time		tSHSL	tCS	30	-	ns
CE# Active setup/hold time relative to SCK		tSLCH/tCHSH	tCSS	3.375	-	ns
CE# Non-Active setup/hold time relative to SCK		tCHSL/tSHCH	tCHS	2.5	-	ns
Output disable time		tSHQZ(3)	tDIS	-	6	ns
Data Input setup time		tDVCH	tSUDAT	2.5	-	ns
Data Input hold time		tCHDX	tHDDAT	1.75	-	ns
Clock LOW to output valid	15pF	tCLQV	tV	-	6	ns
	10pF			-	5	ns
Output hold time	15pF	tCLQX	tHO	2.0	-	ns
	10pF			1.5	-	ns
Hold# setup time (relative to SCK)		tHLCH	tHD	3.375	-	ns
Hold# non-active hold time (relative to SCK)		tCHHH	tCD	3.375	-	ns
Hold# non-active setup time (relative to SCK)		tHHCH	tHC	3.3754.3	-	ns
Hold# hold time (relative to SCK)		tCHHL	tCH	3.3754.3	-	ns
Hold# High to Output Low-Z		tHHQX (3)	tLZ	-	7	ns
Hold# Low to Output High-Z		tHLQZ (3)	tHZ	-	7	ns
WP# setup time		tWHSL	tWPS	20	-	ns
WP# hold time		tSHWL	tWPH	100	-	ns

Notes:

1. Typical values are given for TA = 25°C, V_{CC} = 3.3V.
2. tCH + tCL must add up to 1/fC; 45% - 55% duty cycle is considered.
3. Values are guaranteed by characterization, not 100% tested in production.

5.7 PROGRAM/READ/ERASE CHARACTERISTICS

Parameter		Symbol	Typ	Max	Unit
BLOCK ERASE operation time		tERS	4	10	ms
PROGRAM PAGE operation time	Internal ECC disabled	tPROG (2)	270	600	us
	Internal ECC enabled		320	800	
Page read time	Internal ECC disabled	tRD	-	25	us
	Internal ECC enabled		-	95	
Power-on reset time (Device initialization) from Vcc Min		tPOR	-	2.0	ms
Reset time for READ, PROGRAM, and ERASE operations		tRST	-	10/15/300	us
Number of partial-page programming operations		NOP (1)	-	4	-

Notes:

1. Four total partial-page programs per page. If Internal ECC is enabled, the device is limited to one partial-page program per ECC user area, not exceeding four partial-page programs per page.
2. This protection command execution time also.

6. Security

6.1 VOLATILE BLOCK PROTECTION

The volatile block Protect bits (BP2, BP1, BP0), Inert bit (INV) and Complementary bit (CMP) in block lock register allow part of the memory or entire array to be configured as read-only. The default value for the BP bits, INV bit, and CMP bit are “1” after power up to protect the entire array.

The BP bits, INV bit, and CMP bit cannot be changed by SET FEATURE command when the BRWD bit is set to “1” and WP# pin is driven LOW (Hardware protected mode).
Also, when a PROGRAM/ERASE command issued to a locked block, a status to indicate operation failure is returned. When an ERASE command is issued to a locked block, the erase failure, 04h, is returned.
When a PROGRAM command is issued to a locked block, the program failure, 08h, is returned.

When QE bit is set to ‘1’, this hardware protected mode will be disabled.

Table 6.1 Block Lock Register Block Protect Bits

BP2	BP1	BP0	INV	CMP	Protected Portion
0	0	0	X	X	None – all unlocked
0	0	1	0	0	Upper 1/64 locked
0	1	0	0	0	Upper 1/32 locked
0	1	1	0	0	Upper 1/16 locked
1	0	0	0	0	Upper 1/8 locked
1	0	1	0	0	Upper 1/4 locked
1	1	0	0	0	Upper 1/2 locked
1	1	1	X	X	All locked (default)
0	0	1	1	0	Lower 1/64 locked
0	1	0	1	0	Lower 1/32 locked
0	1	1	1	0	Lower 1/16 locked
1	0	0	1	0	Lower 1/8 locked
1	0	1	1	0	Lower 1/4 locked
1	1	0	1	0	Lower 1/2 locked
0	0	1	0	1	Lower 63/64 locked
0	1	0	0	1	Lower 31/32 locked
0	1	1	0	1	Lower 15/16 locked
1	0	0	0	1	Lower 7/8 locked
1	0	1	0	1	Lower 3/4 locked
1	1	0	0	1	Block 0
0	0	1	1	1	Upper 63/64 locked
0	1	0	1	1	Upper 31/32 locked
0	1	1	1	1	Upper 15/16 locked
1	0	0	1	1	Upper 7/8 locked
1	0	1	1	1	Upper 3/4 locked
1	1	0	1	1	Block 0

For example, if all blocks need to be unlocked after device initialization, the following sequence should be performed.

- Issue SET FEATURE command (1Fh)
- Issue the feature address to unlock the block (A0h)
- Issue 00h on the data bus to unlock all blocks

6.2 HARDWARE WRITE PROTECTION

Hardware write protection prevents the block protection state from hardware modifications.

In order to utilize this feature, SET FEATURE command is issued on the feature address A0h and WP#/HOLD# disable bit state is set to 0.

The BRWD bit is operated in conjunction with WP# signal. When BRWD is set to 1 and WP# is LOW, the device is in the hardware protected mode, none of the other block register bits [7:2] can be set.

The default value of BRWD is “0” after power up.

When QE is set to “1”, hardware protected mode is disabled.

6.3 LOCK TIGHT BIT

The Lock Tight bit prevents locked blocks from being unlocked and also prevents unlocked blocks from being locked.
Once Lock Tight bit is enabled, this mode cannot be disabled via a software command and BP bits, INV and CMP bit and BRWD is protected from further software change.

Once Lock Tight bit is set to “1”, only another power cycle can change this bit to “0” state.

- Issue SET FEATURE command (1Fh)
- Issue the feature address to configuration register bits (B0h)
- Issue 20h on the data bus to enable all Lock Tight bit.

Lock Tight bit provides software protection to protect BP bits, INV, and CMP bit when hardware protection mode is disabled for Quad operations (QE bit = 1).

6.4 PERMANENT BLOCK LOCK PROTECTION (2CH)

Twelve groups of blocks can be permanently locked using PROTECT command. The PROTECT command provides **nonvolatile, irreversible protection** of up to twelve groups (24 blocks in 1Gb, 48 blocks in 2Gb, and also called as boot blocks).

Implementation of the protection is group-based, which means that a minimum of one group (2 blocks in 1Gb, 4 blocks in 2Gb) is protected when PROTECT command is issued.

The device is shipped from the factory with no blocks protected so that users can program or erase the blocks before issuing the PROTECT command. Block protection is also irreversible in that when protection is enabled by issuing the PROTECT command, the protected blocks can no longer be programmed or erased.

If Boot block lock protection disable mode is enabled, PROTECT command would be ignored.

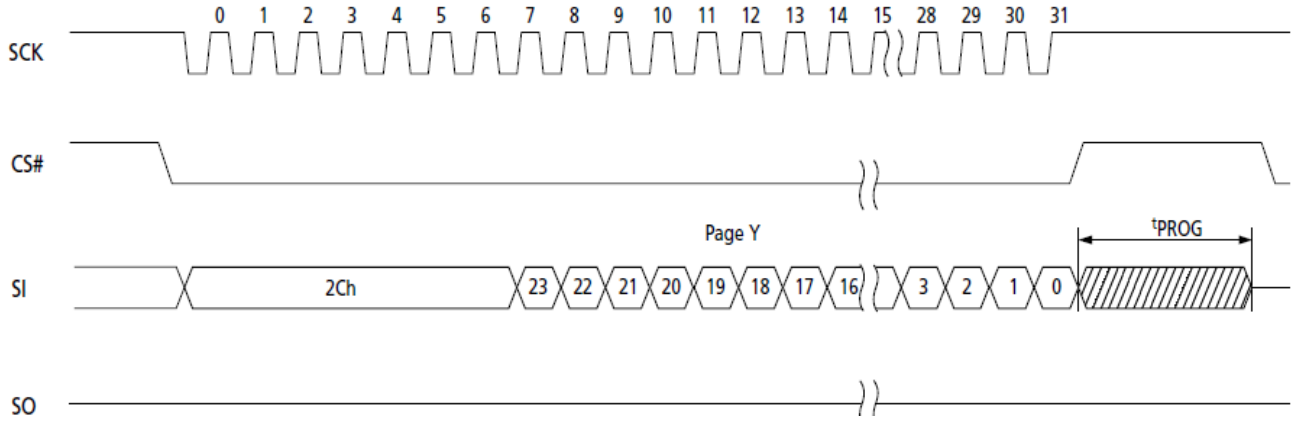
As with any command that changes the memory contents, the WRITE ENABLE must be executed. If this command is not issued, then the protection command is ignored. WRITE ENABLE must be followed by a PROTECTION command (2Ch)

PROTECT SEQUENCE

- 06h (WRITE ENABLE)
- 2Ch (PERMANENT BLOCK LOCK PROTECTION)
- 24-bit address (8 dummy bits and 16-bit page/block address for 1Gb 7 dummy bits and 17-bit page/block address for 2Gb)
- After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P_FAIL bit.

After the page/block address is registered, the corresponding boot block protection bit would be programmed **to lock corresponding boot block group.**

Figure 6.1 PROTECT command Cycle



PERMANENT BLOCK LOCK PROTECTION COMMAND (2Ch) Details

To enable protection, the PROTECTION command consists of an 8-bit command code (2Ch), followed by a 24-bit address (8 dummy bits +16-bit valid page block address in 1Gb, 7 dummy bits +17-bit valid page block address in 2Gb). Row address bits 11, 10, 9, 8 (named as Y) input the targeted block group information. When Y defines the group of blocks to be protected. There are 12 Groups Y where Y= 0000b – 1011b.

- Y=0000 protect Group 0 = block 0, 1, 2, 3.
- Y=0001 protect Group 1 = block 5, 6, 7, 8.
- ….
- Y=1011 protect Group 11 = block 44, 45, 46, 47.

After tPROG, the targeted block groups are protected. Upon PROTECT operation failure, the status register reports a value of 08h (P_FAIL = 1). Upon PROTECT operation success, the status register reports a value of 00h.

Note: There is no status register to check the PROTECT status of a block or a group. A permanent blocks table should be maintained and updated after a group is protected.

6.5 ONE TIME PROGRAMMABLE (OTP)

This device offers a protected, one-time programmable memory area. Ten full pages (2176 or 2112 bytes per page) are available, and the entire range is guaranteed to be good. Customers can choose how to use the OTP area, such as programming serial numbers or other data for permanent storage.
The OTP area leaves the factory in an erased state (all bits are 1). The OTP area can't be erased once programmed.

When Internal ECC is enabled, data written in the OTP area is ECC protected.

ENABLE OTP Access.

The OTP area is accessible while the OTP operation mode is enabled. To enable OTP operation mode, issue SET FEATURE command (1Fh) to feature address B0h and data value of 40h (OTP operation mode and Internal ECC disable) or 50h (OTP operation mode and Internal ECC enable).

When the device is in OTP operation mode, all subsequent PAGE PROGRAM or PAGE READ commands are applied to the OTP area. Erase commands are not valid while the device is in OTP operation mode.

Table 6.2 OTP Configuration States

OTP_CFG2	OTP_CFG1	OTP_CFG0	State
0	0	0	Normal Operation
0	0	1	Normal Operation (Reserved)
0	**1**	**0**	Access OTP area / Parameter page / Unique ID (named as OTP operation mode)
0	1	1	Normal Operation (Reserved)
1	0	0	Normal Operation (Reserved)
1	0	1	Normal Operation (Reserved)
1	**1**	**0**	Access OTP Data Protection bit to lock OTP area (named as OTP DATA protection mode)
1	**1**	**1**	Access to Disable Boot Block Lock Protection (named as Boot block lock protection disable mode)

Each page in the OTP area can be programmed using the PAGE PROGRAM sequence. Each page can be programmed more than once up to the maximum number allowed. By reading P_FAIL bit of the status register, program operation passed or failed could be determined.

If the host attempts to program the OTP pages which are out of bounds, program command will be ignored and P_FAIL bit = 1 will be reported.

If the host attempts to program the OTP pages after OTP area is protected, the program command will be ignored and P_FAIL bit = 1 will be reported.

To read pages in the OTP area, whether the OTP area is protected or not, issue the PAGE READ sequence.

If the host issues the PAGE READ (13h) command to an address beyond maximum page-address range, the data output will not be valid. To determine whether the device is busy during an OTP operation, use GET FEATURE (0Fh) command at feature address C0h to check OIP bit.

To exit from OTP operation mode and return to normal array operation mode, issue SET FEATURE (1Fh) command with feature address B0h and data value of 00h or 10h.

If the RESET (FFh) command is issued while in OTP operation mode, the device will exit OTP operation mode and enter normal operation mode.

In OTP operation mode, page address 00h is to read out UniqueID page; page address 01h is to read out parameter page.

After OTP access is enabled, the following sequence is used to program one or more pages

- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with the row address of page (OTP page address range 02h-0Bh)
- Verify until OIP bit not busy using GET FEATURE command (0Fh) with feature address C0h
- Using GET FEATURE command (0Fh) with feature address C0h to verify P_FAIL bit is 0 for the successful operation.

After OTP access is enabled, the following sequence is used to read one or more pages

- PAGE READ command (13h) with the page address (02h-0Bh)
- Verify until OIP bit not busy using GET FEATURE command (0Fh) with feature address C0h
- Page data using READ FROM CACHE command (03h).

OTP DATA PROTECT

OTP DATA PROTECT mode is used to prevent further programming of pages in the OTP area. In OTP DATA PROTECT mode, the following program sequence is used to enable OTP DATA PROTECT mode:

- SET FEATURE command (1Fh) with feature address B0h and data value of C0h (access OTP DATA PROTECT mode)
- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with block/page address all '0'.
- GET FEATURE command (0Fh) with feature address C0h (status register address) to check if the device is ready or busy (OIP bit)
- Using GET FEATURE command (0Fh) with feature address C0h to verify P_FAIL bit is 0 for the successful operation

If the program sequenced again after the OTP area has already been protected, program command will be ignored, the status register is set to 00h.

Boot Block Lock Protection Disable

Boot block lock protection disable mode is used to prevent further adding non-volatile locked block groups by protection command. In Boot block lock protection disable mode, the following program sequence is used to disable protection command to add more non-volatile locked block groups:

- SET FEATURE command (1Fh) with feature address B0h and data value of C2h (access Boot Block lock protection disable mode)
- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with block/page address all '0'.
- PAGE READ command (13h) with address 0
- Using GET FEATURE command (0Fh) with feature address C0h to verify P_FAIL bit is 0 for the successful operation

If the program sequenced again after boot block lock protection is disabled, program command will be ignored, the status register is set to 00h.

7. IDENTIFIVATION OPERATIONS

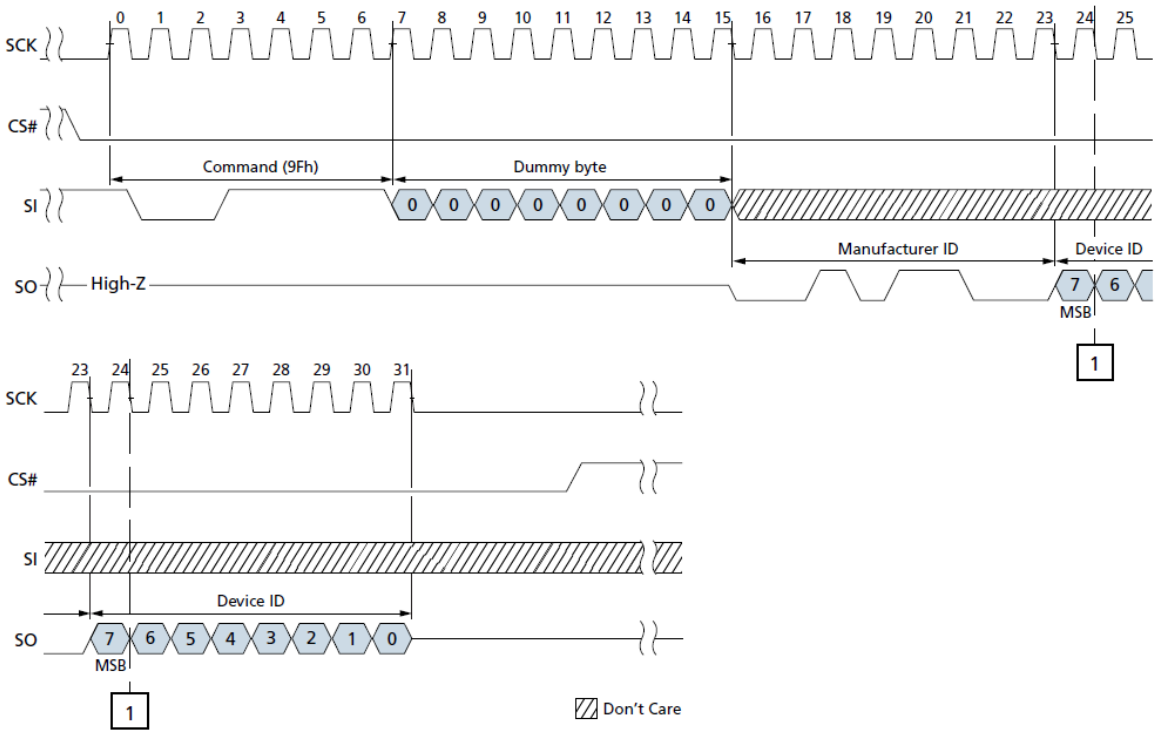
7.1 READ ID

READ ID reads the 2-byte identifier code programmed into the device, which includes ID and device configuration data as shown in the table below.

Table 7.1 READ ID Table

Byte	Description	7	6	5	4	3	2	1	0	Value
Byte 0	Manufacturer ID	1	0	0	1	1	1	0	1	9Dh
Byte 1	1Gb 3.3V Device ID	0	0	0	1	0	1	0	0	14h
	2Gb 3.3V Device ID	0	0	1	0	0	1	0	0	24h

Figure 7.1 READ ID (9Fh) Timing



7.2 PARAMETER PAGE

The following command flow must be issued by the memory controller to access the parameter page:

1. 1Fh - SET FEATURE command with a feature address of B0h and data value 40h to access OTP/Parameter/Unique ID pages, ECC disable).
2. 13h - PAGE READ command with a block/page address of 0x01h, and then check the status of the read completion using GET FEATURE (0Fh) command with a feature address of C0h.
3. 03h - READ FROM CACHE COMMAND with an address of 0x00h to read the data out of the device
4. 1Fh – SET FEATURE command with a feature address of B0h and data value of 10h or 00h (main array READ, ECC enable/disable).

7.3 PARAMETER PAGE DATA STRUCTURE

Table 7.3 Parameter Page Data Structure

Revision Information and Feature Block				
Byte	**Description**			**Value**
0-3	Parameter page signature			4Fh, 4Eh, 46h, 49h
4-5	Revision number			00h, 00h
6-7	Feature supported			00h, 00h
8-9	Optional commands supported			24h, 00h
	15-6: Reserved (0)			
	5: 1 = supports Read Unique ID			
	4: 1 = supports Copy back			
	3: 1 = supports Read Status Enhanced			
	2: 1 = supports Get Feature and Set Feature			
	1: 1 = supports Read Cache commands			
	0: 1 = supports Page Cache Program command			
10-31	Reserved			00h
Manufacturer Information Block				
32-43	Device manufacturer (12 ASCII characteristics)			49h, 53h, 53h, 49h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device Model	1Gb, 3.3V	IS37SML01G8B	49h, 53h, 33h, 37h, 53h, 4Dh, 4Ch, 30h, 31h, 47h, 38h, 42h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		2Gb, 3.3V	IS37SML02G8B	49h, 53h, 33h, 37h, 53h, 4Dh, 4Ch, 30h, 32h, 47h, 38h, 42h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID			9Dh
65-66	Date Code			00h, 00h
67-79	Reserved			00h
Memory Organization				
Byte	**Description**			**Value**
80-83	Number of Data Bytes per Page			00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page			80h, 00h (ECC Off)
86-89	Number of Data Bytes per Partial Page			00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page			20h, 00h (ECC Off)
92-95	Number of Pages per Block			40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		1Gb	00h, 04h, 00h, 00h
			2Gb	00h, 08h, 00h, 00h
100	Number of logical units		1Gb	01h
			2Gb	01h

101	Number of address cycles (NA)		00h
102	Number of bits per cell		01h
103-104	Bad blocks maximum per unit	1Gb	14h, 00h
		2Gb	28h, 00h
105-106	Block Endurance		01h, 05h
107	Guaranteed Valid Blocks at Beginning of Target		08h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of program per page		04h
111	Partial programming attributes		00h
112	Number of ECC bits		00h
113	Number of interleaved address bits		00h (N/A)
114	Interleaved operation attributes		00h (N/A)
115-127	Reserved		00h
Electrical Parameters Block			
Byte	**Description**		**Value**
128	I/O pin capacitance		0Ah
			0Ah
129-130	Timing mode support		00h, 00h (NA)
131-132	Program cache timing mode support		00h, 00h (NA)
133-134	tPROG (MAX) page program time (uS)	800us	20h, 03h
135-136	tBERS (MAX) block erase time (uS)	10000us	10h, 27h
137-138	tR_maximum page read time (uS)	25us	19h, 00h
139-163	Reserved		00h
Vendor Blocks			
Byte	**Description**		**Value**
164-165	Vendor-specific revision number		00h, 00h (NA)
166-179	Vendor-specific		00h
180-247	Reserved		00h
248	ECC maximum correct ability		08h
249-253	Reserved		00h
254-255	Integrity CRC (1)		Set at Test
256-511	2nd copy of the parameter table		
512-767	3rd copy of the parameter table		
768+	Additional redundant parameter pages		

Note:

1. The integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host. The CRC shall be calculated using the following 16-bit generator polynomial: G(X) = X16 + X15 + X2 + 1

8. DEVICE OPERATION

7.4 UNIQUE ID PAGE

The following command flow must be issued by the memory controller to access the unique ID page contained within the device:

1. 1Fh - SET FEATURE command with a feature address of B0h and data value for 40h (to access OTP/Parameter/Unique ID pages/ECC Disable).
2. 13h - PAGE READ command with a block/page address of 0x00h, and then check the status of read completion using GET FEATURE (0Fh) command with a feature address of C0h.
3. 03h - READ FROM CACHE COMMAND with an address of 0x00h to read the Unique ID data out of the NAND device
4. 1Fh – SET FEATURE command with a feature address of B0h and data value of 10h or 00h (main array READ, ECC enable/disable) to exit Unique ID reading.

The device stores 16 copies of the Unique ID data. Each copy is 32 bytes: the first 16 bytes are unique data, and the second 16 bytes are the complement of the first 16 bytes.

The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, that copy of Unique ID data is correct. If a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the Unique ID data.

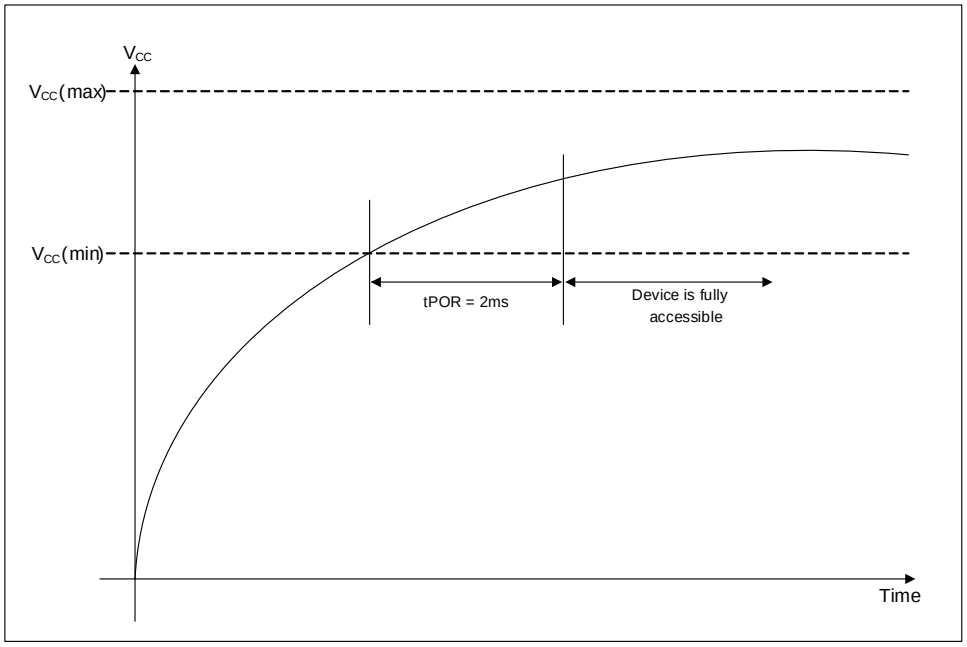
8.1 POWER-UP SEQUENCE

POWER UP Sequence

The device is designed to prevent data corruption during power transitions. VCC is internally monitored and when VCC reaches 2.5V, the device automatically performs the device initialization. The first page data would be automatically loaded into the cache register.

The first access to the device can occur at tPOR (2ms) after VCC reaches VCC min (2.7V) and then C# can be driven LOW, SCK can start, and the required command can be issued to the device.
Note that CS# must track the VCC supply level during power up until VCC reaches to VCC min. If needed, a pull-up resister on the CS# can be used to accomplish this.

Figure 8.1 Power-Up Sequence



POWER DOWN Sequence

Upon power-down, the device requires a maximum voltage and minimum time that the host should hold VCC below the voltage prior to power on. Note that CS# must also track the VCC level during power down to prevent adverse command sequence.

Parameter	Value	Unit
Power-Down Maximum VCC	100	mV
Minimum Time below Power-Down Maximum VCC	100	ns

Note:

1. VCC Slew Rate:1.0 mV/us < ramp rate < 50.0 mV/us.

8.2 RESET (FFH)

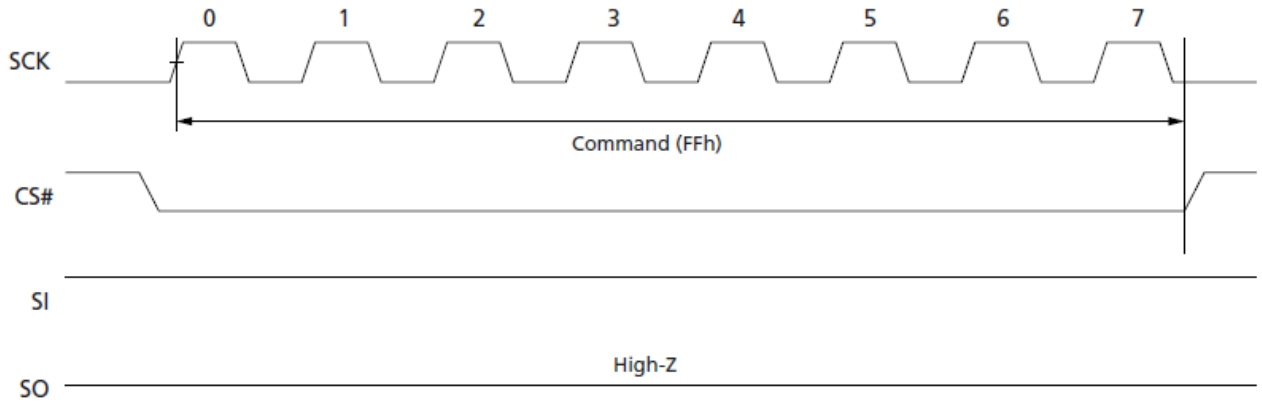
The RESET command (FFh) is used to put the memory into a known condition and to abort the command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be protially erased or programmed, and is invalid. The status register bits are cleared. RESET command also reset OTP_CFG2, 1, 0 (One Time Programmable Configuration Register Bits) back to normal. **While all other configuration register bits will not be reset.**

The block lock register bits will not be cleared after reset. **The block lock register bits will be cleared by POWER CYCLE or writing SET FEATURE command.**

Once the RESET command is issued to the device, it will take tRST to complete reset operation. During this period, the GET FEATURE command can be issued to monitor the status (OIP). While the device is busy after sending RESET command, READ ID command can be issued to read device ID.

Figure 8.2 RESET (FFh) Timing



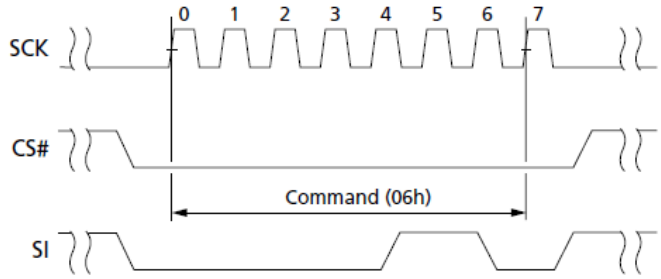
8.3 WRITE OPERATIONS

WRITE ENABLE (06h)

The WRITE ENABLE (06h) command sets the WEL bit in the status register to 1. WRITE ENABLE is required in the following operations that change the contents of the memory array:

- **PAGE PROGRAM**
- **OTP AREA PROGRAM**
- **BLOCK ERASE**

Figure 8.3 WRITE ENABLE (06h) Timing

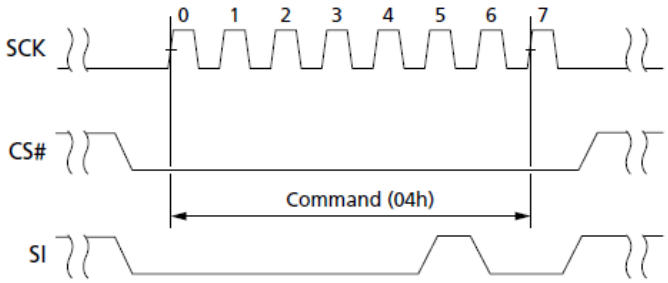


WRITE DISABLE (04h)

The WRITE DISABLE (04h) command clears the WEL bit in the status register to 0. Disabling the following operations:

- **PAGE PROGRAM**
- **OTP AREA PROGRAM**
- **BLOCK ERASE**

Figure 8.4 WRITE DISABLE (04h) Timing



8.4 ADDRESS REQUIREMENT

The device requires 24-bit address or 16-bit address for read, program, erase, and protection operations.

Command requires 24-bit address: PAGE READ (13h), READ PAGE CACHE RANDOM (30h), PROGRAM EXECUTE (10h), BLOCK ERASE (D8h), PERMANENT BLOCK LOCK PROTECTION (2Ch)

Command requires 16-bit address: READ FROM CACHE x1 (03h/0Bh), READ FROM CACHE x2 (3Bh), READ FROM CACHE x4 (6Bh), PROGRAM LOAD x1 (02h), PROGRAM LOAD x4 (32h), PROGRAM LOAD RANDOM DATA x1 (84h), PROGRAM LOAD RANDOM DATA x4 (34h)

- **24-bit address is consist of dummy bits + valid block/page address like table 8.1.**

Table 8.1 24-bit Address Table

Density	Dummy bits	Valid block/page Address	Total (bit)
1Gb	8	RA[15:6] , 16 address	24
2Gb	7	RA[16:6], 17 address	24

- **16 bit address is consist of dummy bits +12 column address**

Table 8.2 16 bit Address Table

Density	Dummy Bits	Column Address	Total (bit)
1Gb	4	CA [11:0], 12 address	16
2Gb	4		16

8.5 PAGE READ OPERATION

The PAGE READ (13h) command transfers data from the cell array to the cache register. It requires a 24-bit address (8 dummy bits for 1Gb/ 7 dummy bits for 2Gb + 16-bit/17-bit valid block/page address).

After the 24-bit address is registered, the device starts the transfer from main array to the cache register. During this data transfer busy time of tRD, the GET FEATURE command can be issued to monitor the operation.

Following successful completion of PAGE READ, the READ FROM CACHE command must be issued to read data out of cache. The command sequence is as follows to transfer data from array to output:

13h (PAGE READ command to cache register)

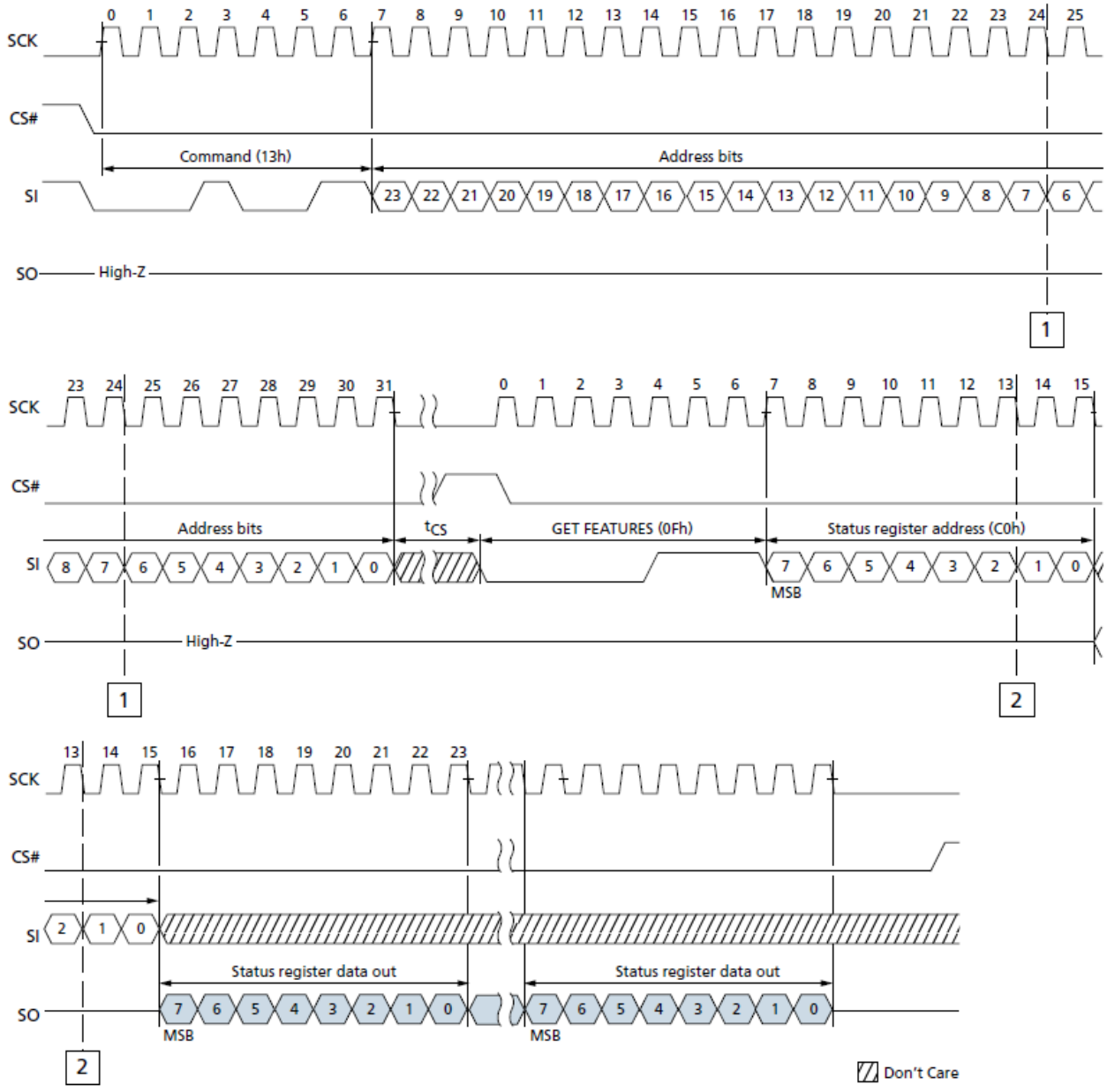
0Fh (GET FEATURE command to read the status)

03h or 0Bh (READ FROM CACHE): 1-1-1 READ

3Bh (READ FROM CACHE x2): 1-1-2 READ

6Bh (READ FROM CACHE x4): 1-1-4 READ

Figure 8.5 PAGE READ (13h) and GET FEATURE (0Fh) Timing

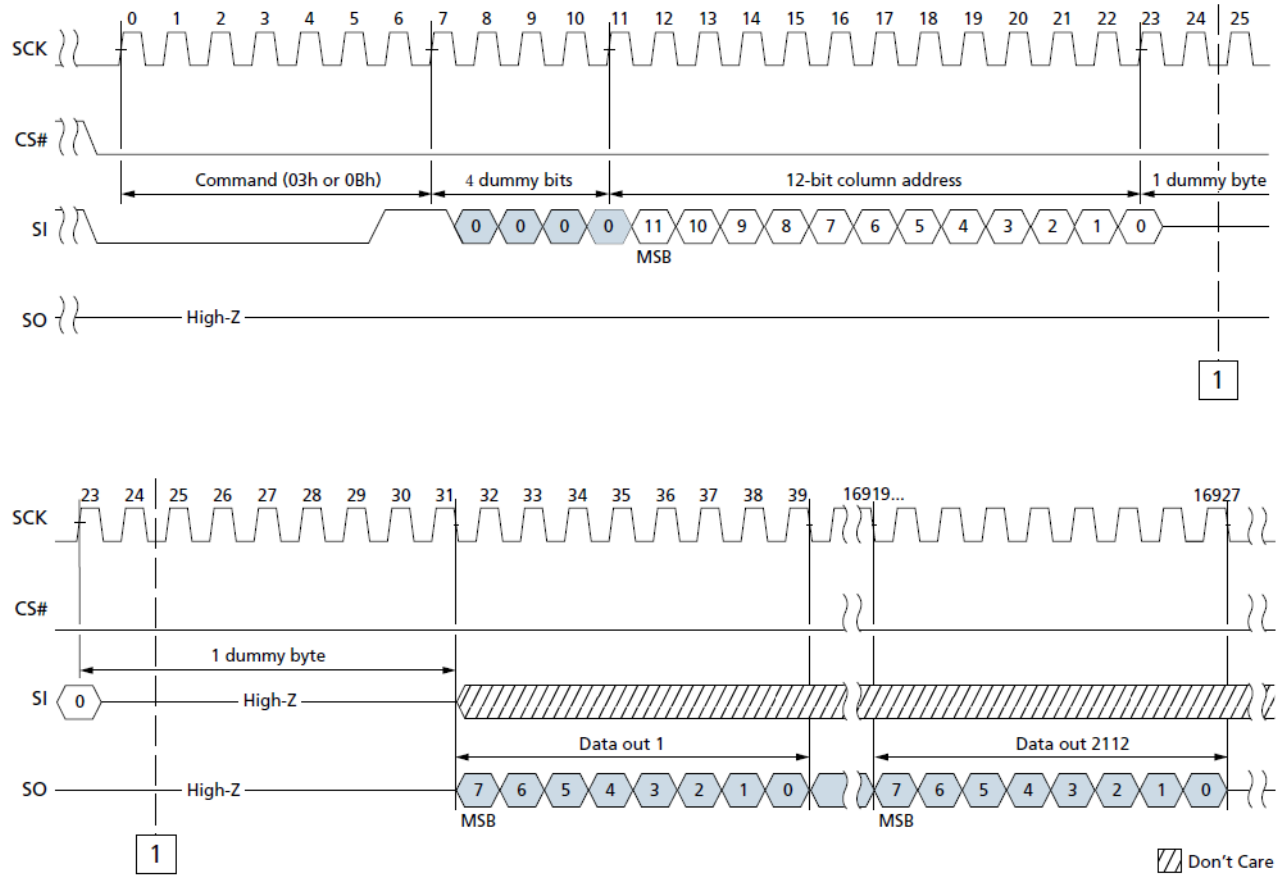


8.6 READ FROM CACHE X1 (03H OR 0BH)

The READ FROM CACHE x1 command (03h or 0Bh) enables sequentially reading one or more data bytes from the cache buffer. The command is initiated by driving CS# LOW, shifting in command opcode 03h/0Bh, followed by a 16-bit address (4 dummy bits + 12 column address).

Data is returned after 8 dummy clocks from the addressed cache buffer, MSB first, on SO at the falling edge of SCK. The address is automatically incremented to the next higher address after each byte of data shifted out, enabling a continuous stream of data. This command is completed by driving CS# HIGH.

Figure 8.6 READ from CACHE x1 (03h or 0Bh) Timing



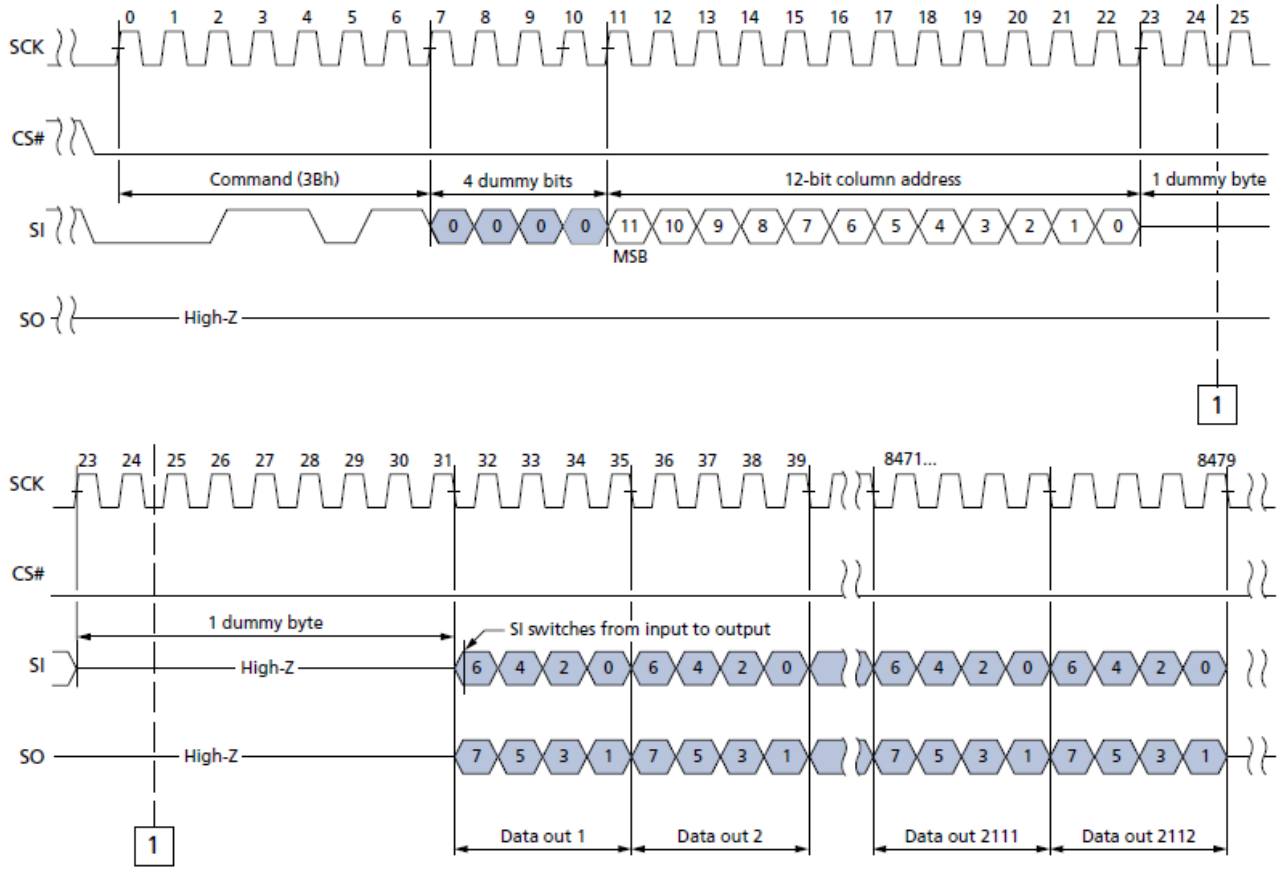
Note:

1. Last Data out will be 2176 when ECC is disabled.

8.7 READ FROM CACHE X2 (3BH)

The READ FROM CACHE x2 (3Bh) command is similar to READ FROM CACHE x1 (03h or 0Bh) except that output data is transferred through two pins; IO0 (SI) and IO1 (SO). This allows data to be transferred at twice the rate of 03h/0Bh command.

Figure 8.7 READ from CACHE x2 (3Bh) Timing



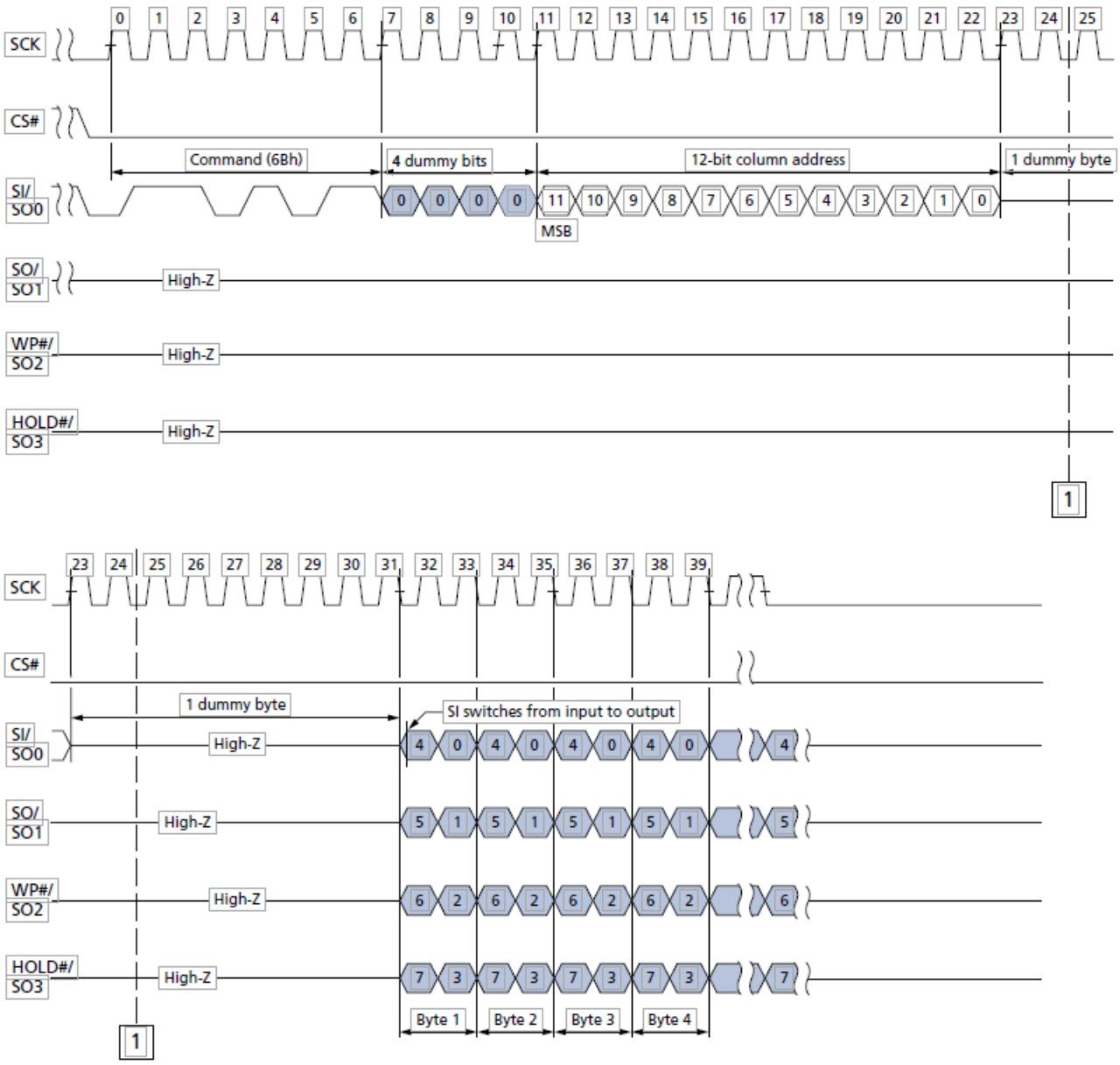
Note:

1. Last Data out will be 2176 when ECC is disabled.

8.8 READ FROM CACHE X4 (6BH)

The READ FROM CACHE x4 (6Bh) command is similar to READ FROM CACHE x1 (03h or 0Bh) except that output data is transferred through four pins (IO0~IO3). This allows output data to be transferred at four times the rate of 03h/0Bh command.

Figure 8.8 READ from CACHE x4 (6Bh) Timing



8.9 PAGE PROGRAM OPERATIONS

A PAGE PROGRAM operation sequence enables the host to input 1 byte to 2176 or 2112 bytes of data within a page.

- **If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register**

The page program sequence is as follows:

- 06h (Write Enable command)
- 02h (Program Load command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURE command to read the status)

8.10 PROGRAM LOAD X1 (02H)

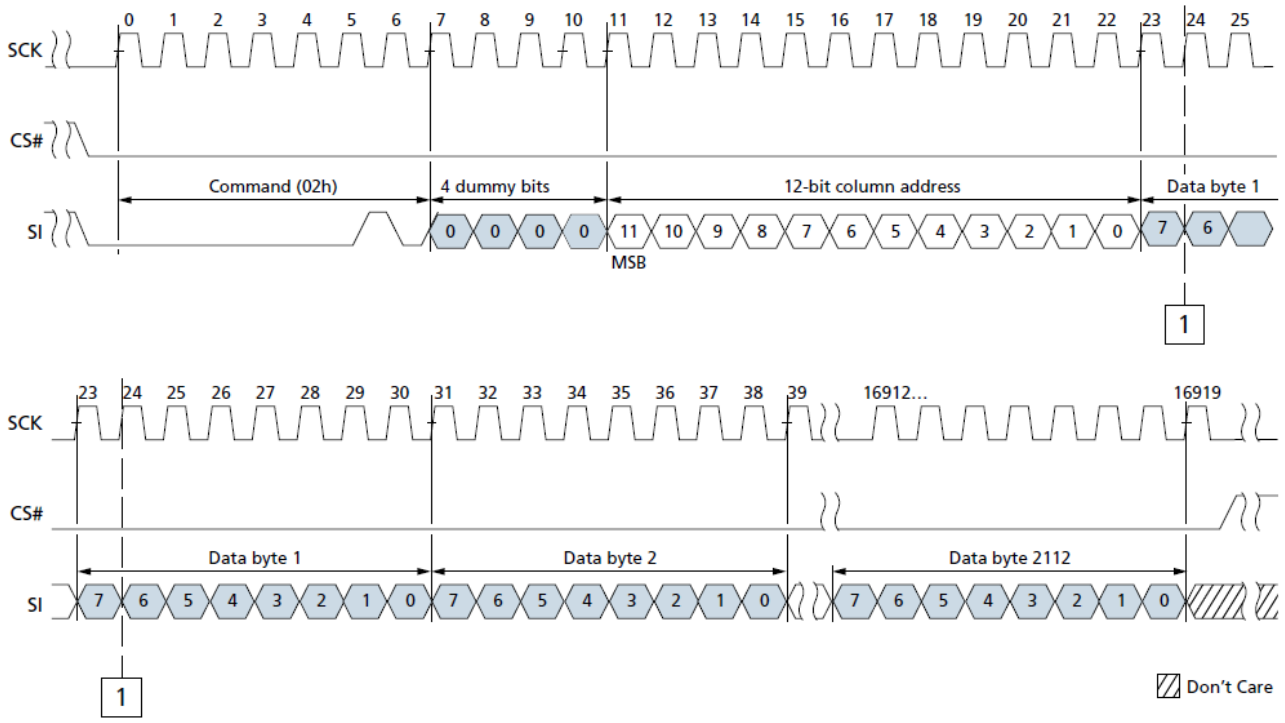
Prior to performing PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be issued in order to set WEL bit. WRITE ENABLE is followed by a PROGRAM LOAD (02h) command.

The PROGRAM LOAD command consists of an 8-bit opcode, followed by 16 bit address (4 dummy bits + 12 column address), and then the data bytes to be programmed.

The data bytes are loaded into a cache register that is 2176 or 2112 bytes long. **Only four partial page programs are allowed on a single page.**

The command sequence ends when CS# goes from LOW to HIGH.

Figure 8.9 PROGRAM LOAD x1 (02h) Timing



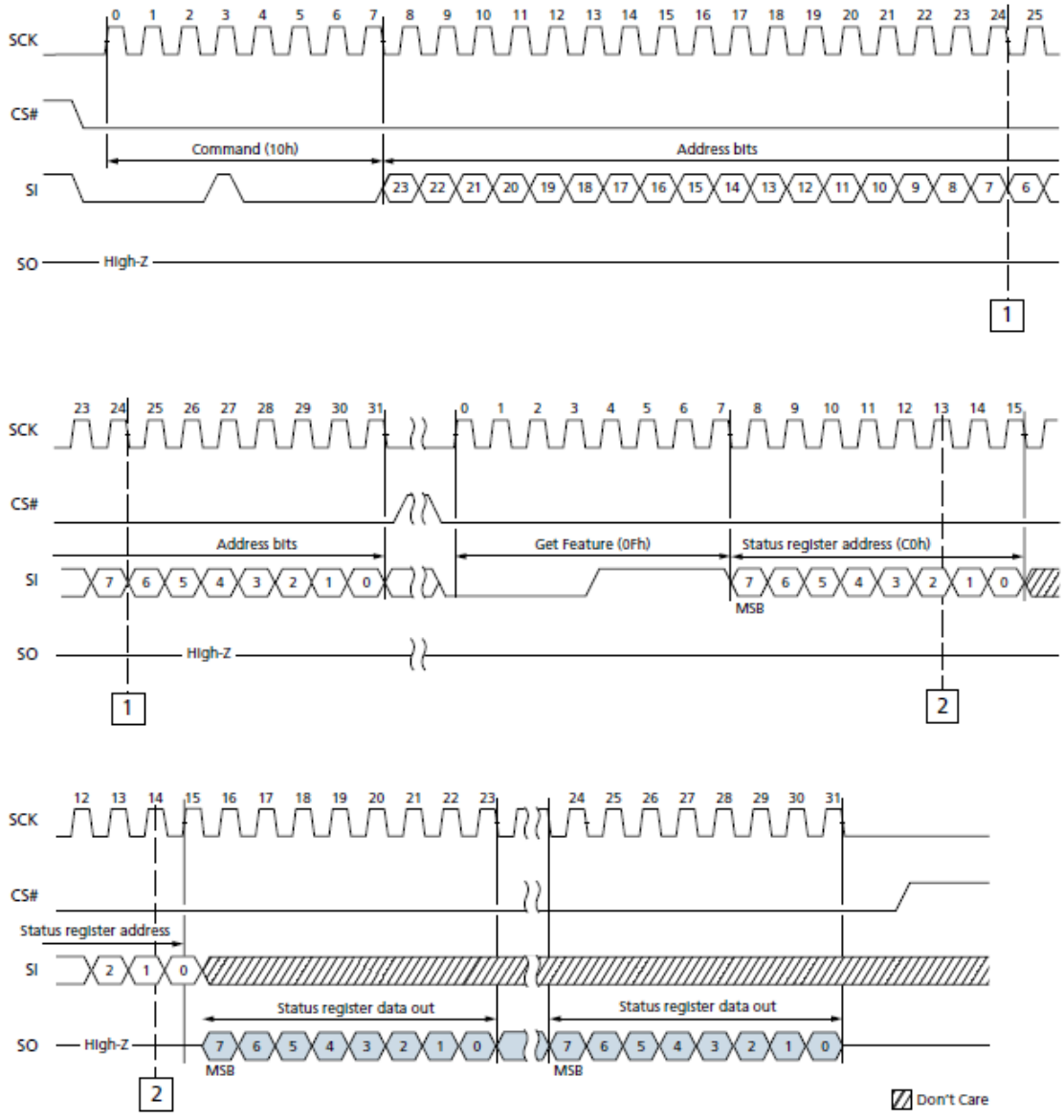
8.11 PROGRAM EXECUTE (10H)

The PROGRAM EXECUTE command consists of an 8-bit op code, followed by a 24-bit address (dummy bits + valid page/block address - 16 addresses for 1Gb, 17 addresses for 2Gb).

After the page/block address is registered, **the device starts the transfer from the cache register to the main array** and is busy for tPROG time.

During this busy time, the status register can be polled to monitor the status of the operation. When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure 8.10 PROGRAM EXECUTE TIMING



8.12 RANDOM DATA PROGRAM X1 (84H)

The RANDOM DATA PROGRAM sequence programs or replaces data in a page with existing data. The RANDOM DATA PROGRAM sequence is as follows:

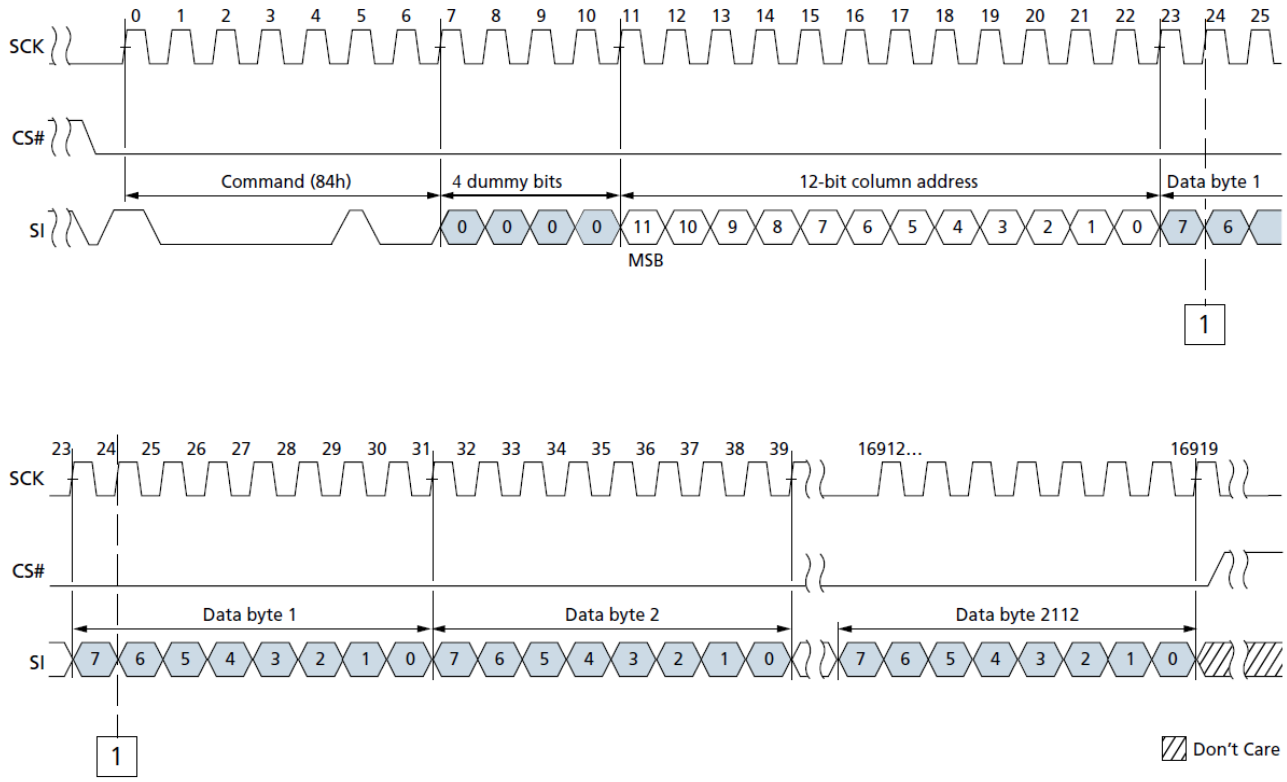
- 06h (WRITE ENABLE command)
- **84h (PROGRAM LOAD RANDOM DATA command)**
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURE command to read the status)

The PROGRAM LOAD RANDOM DATA x1 (84h) operation is similar to PROGRAM LOAD x1 (02h).

The PROGRAM LOAD RANDOM DATA x1 (84h) command consists of an 8-byte Op code, followed by 4 dummy bits, followed 12-bit column address. New data is loaded in the column address provided with the 12-bit column address. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA x1 (84h) command must be issued with a new column address. After data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

The difference is that PROGRAM LOAD x1 command will reset cache buffer to an all FFh value, while RANDOM LOAD x1 command will only update the data bytes that are specified by the command input sequence, and the rest of data in the cache buffer will remain unchanged.

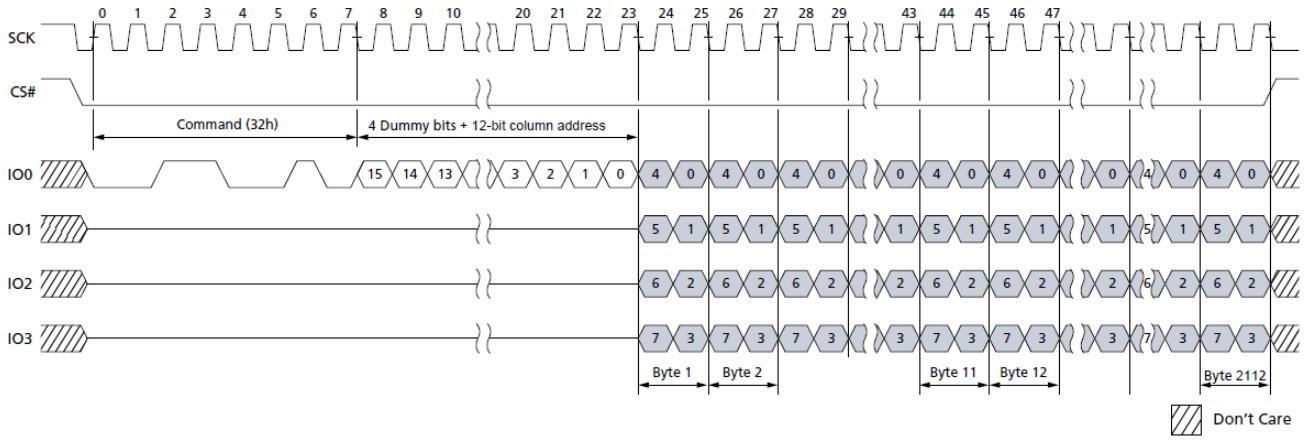
Figure 8.11 PROGRAM LOAD RANDOM DATA (84h) Timing



8.13 PROGRAM LOAD X4 (32H) AND PROGRAM LOAD RANDOM DATA X4 (34H)

The PROGRAM LAOD x4 (32h) and RANDOM DATA x4 (34h) is similar to PROGRAM LOAD x1 (02h) command and RANDOM DATA x1 (84h), **but with the capability to input the data bytes from all four IO pins instead of the single SI pin.** This will significantly shorten the data input time when a large amount of data needs to be loaded into the cache buffer.

Figure 8.12 PROGRAM LOAD x4 (32h) Timing



8.14 INTERNAL DATA MOVE

The INTERNAL DATA MOVE command programs or replaces data in a page with existing data. The internal data move command sequence is as follows:

- **13h (PAGE READ to cache register)**
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA) or 34h (PROGRAM LOAD RANDOM DATA x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE to read the status)

Prior to performing an internal data move operation, the target page content must be read into the cache register. This is done by issuing a PAGE READ (13h) command. The PAGE READ command must be followed with a WRITE ENABLE (06h) command in order to change the contents of memory array. After the WRITE ENABLE command is issued, the PROGRAM LOAD RANDOM DATA (84h) command or PROGRAM LOAD RANDOM DATA x4 (34h) command can be issued. The command is followed by 4 dummy bits, followed by 12-bit column address. New data is loaded in the 12-bit column address.

Note: If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h) or PROGRAM LOAD RANDOM DATA x4 (34h) must be issued with the new column address.

After the data is loaded, a PROGRAM EXECUTE (10h) command can be issud to start the rogramming operation.

8.15 BLOCK ERASE OPERATIONS

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048 + 128 bytes). Each block is 136 Kbytes. The BLOCK ERASE command (D8h) operations on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

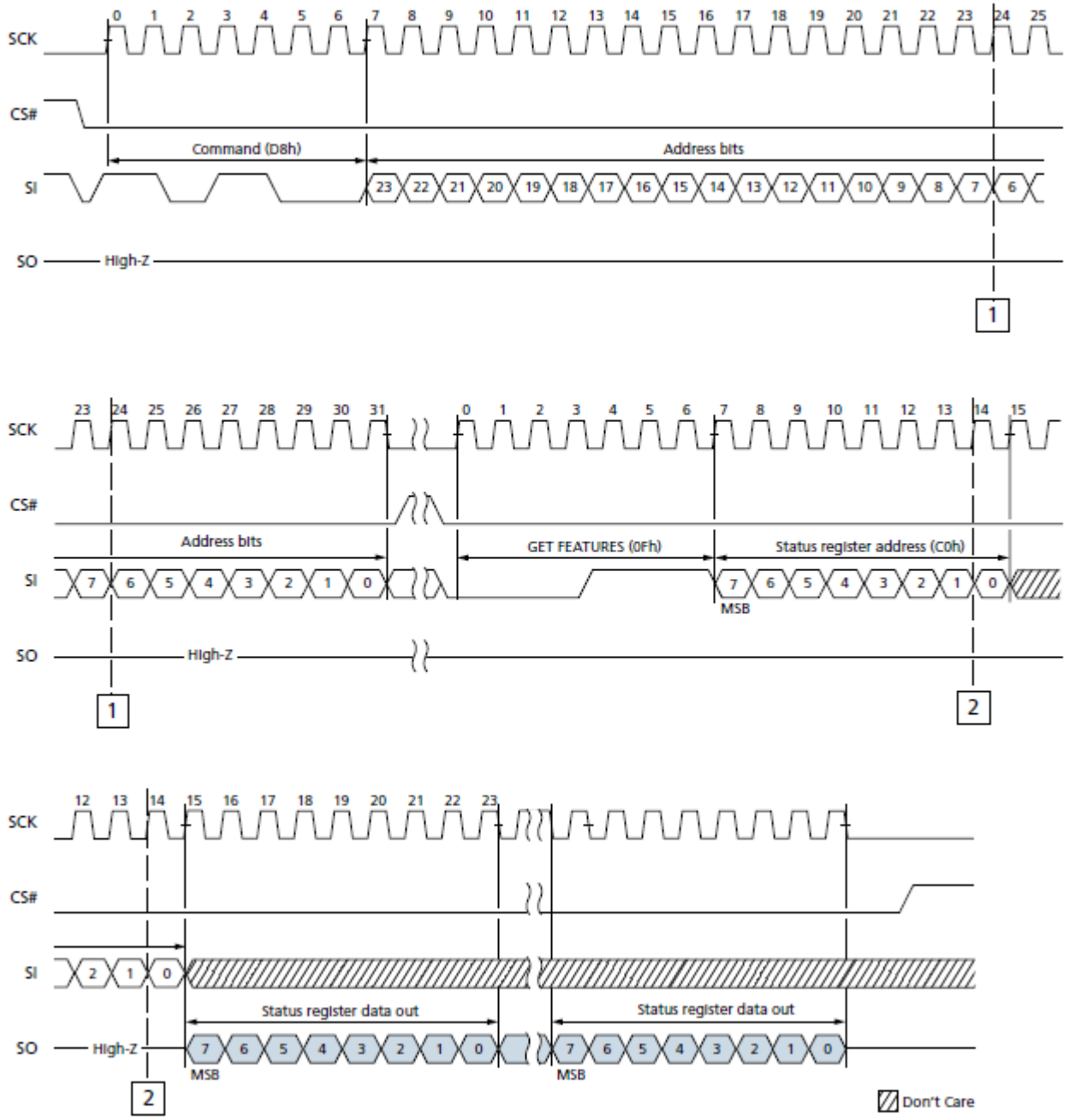
- 06h (WRITE ENABLE command)
- **D8h (BLOCK ERASE command)**
- 0Fh (GET FEATURE command to read the status register).

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit.

If the WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires **24-bit address** consisting of dummy bits and valid block/page address. (8 dummy bits + 16-bit page/block address for 1Gb, 7 dummy bits + 17-bit page/block address for 2Gb)

After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tERS time during the BLOCK ERASE operation. The GET FEATURE (0Fh) command can be used to monitor the status of the operation.

Figure 8.13 BLOCK ERASE (D8h) Timing



8.16 ECC PROTECTION

The device offers data corruption protection by offering 8-bit internal ECC to obtain the data integrity. The internal ECC can be enabled or disabled by ECC bit in the configuration register. **Internal ECC is enabled after power-up by default**. Reset will not change the existing configuration. To enable/disable ECC, perform the following command sequence:

- Issue SET FEATURE command (1Fh)
- Issue configuration register address (B0h)
- Set bit 4 (ECC_ENABLE) to 1 to enable ECC; Clear bit 4 (ECC_ENABLE) to 0 to disable ECC.

During a program operation, the device calculates an expected ECC code on the 2KB page (ECC protected bytes) in the cache register, before the page is written to the Flash array. The ECC code is stored in the spare area of the page.

During a read operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the expected ECC code value read from the array. If a 1 to 8-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status register bit indicates whether or not the error correction is successful.

The Unique ID and parameter page are not ECC protected areas.

Multiple copies are provided for parameter page to obtain the data integrity. XOR method is provided for Unique ID to verify data.

With internal ECC, users must accommodate the following.

- Spare area definitions provided in the ECC Protection table shown Table 8.5, “ECC Protection”.
- ECC protected are supported for main, spare and parity areas 0, 1, 2, and 3. The “main 0” and “Spare 0” are belongs to one ECC sector with “Parity 0” to store its own parity bytes, and same scheme for main and spare 1, 2, 3.

When using partial-page programming, the following conditions must be met:

- In the main user area and user spare area, **single partial-page programming operations must** be used.
- **Within a page, a maximum of four partial-page programming operations can be performed.**

Table 8.4 ECC Status Register Bit Descriptions

Bit 2	Bit 1	Bit 0	ECC Status
0	0	0	No bit error detected during the previous read algorithm.
0	0	1	1-3 bit errors detected and corrected; no data refreshment is required. (1)
0	**1**	**0**	**More than 8 bit errrors detected and not corrected**
0	1	1	4-6 bit errors detected and corrected; data refreshment is recommended. (1)
1	0	0	Reserved
1	0	1	7-8 bit errors detected and corrected; data refreshment must be taken to guarantee data retention (1)
1	1	0	Reserved
1	1	1	Invalid state

Notes:

1. **Bit 0 = 1 indicates 1 to 8-bit errors/sector were detected and corrected.**
2. **If internal ECC is OFF, ECC status should be ignored and user needs to clear ECC status by issuing RESET command after ECC OFF.**

Table 8.5 Spare Area Mapping

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
80Fh	800h	Yes	Spare 0	Spare 0
81Fh	810h	Yes	Spare 1	Spare 1
82Fh	820h	Yes	Spare 2	Spare 2
83Fh	830h	Yes	Spare 3	Spare 3
84Fh	840h	Yes	Parity 0	ECC for main/spare 0
85Fh	850h	Yes	Parity 1	ECC for main/spare 1
86Fh	860h	Yes	Parity 2	ECC for main/spare 2
87Fh	870h	Yes	Parity3	ECC for main/spare 3

8.17 ERROR MANAGEMENT

The NAND Flash is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the device could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per device will not fall below NVB during the endurance life of the product.

Although the device could contain bad blocks, they can be used quite reliably in systems that provide bad block management and error correction algorithms.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the blocks.

The NAND device is shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad block mark into every location in the first and second page of each invalid block.

The first spare area location in each bad block is guaranteed to contain the bad block mark.

Table 8.6 Error Management Details

Description		Requirement	Remark
Minimum number of valid blocks (NVB) per die (LUN)	1Gb	1004	Block 0-7 is guaranteed too be good at the time of shipment (with ECC enabled)
	2Gb	2008	
Total available blocks per die (LUN)	1Gb	1024	
	2Gb	2048	
First spare area location in the first page of each block		Byte 2048th	
Value programmed for **bad block** at the first byte of spare area		00h	

System software should initially check the first spare area location for non-FF data on the first or second page of each block prior to performing any PROGRAM or ERASE operations on the device. A bad block table can then be created, enabling system software to map around these areas.

Note that it may not be possible to recover the bad-block marking if the block is erased.

Additional bad blocks may develop with use over the lifetime. In this case, each bad block has to be replaced by copying any valid data to a new block. These additional bad blocks can be identified by checking ECCS2, 1, 0, P_FAIL and E_FAIL bit in the Status Register, after each read, program, and erase operation.

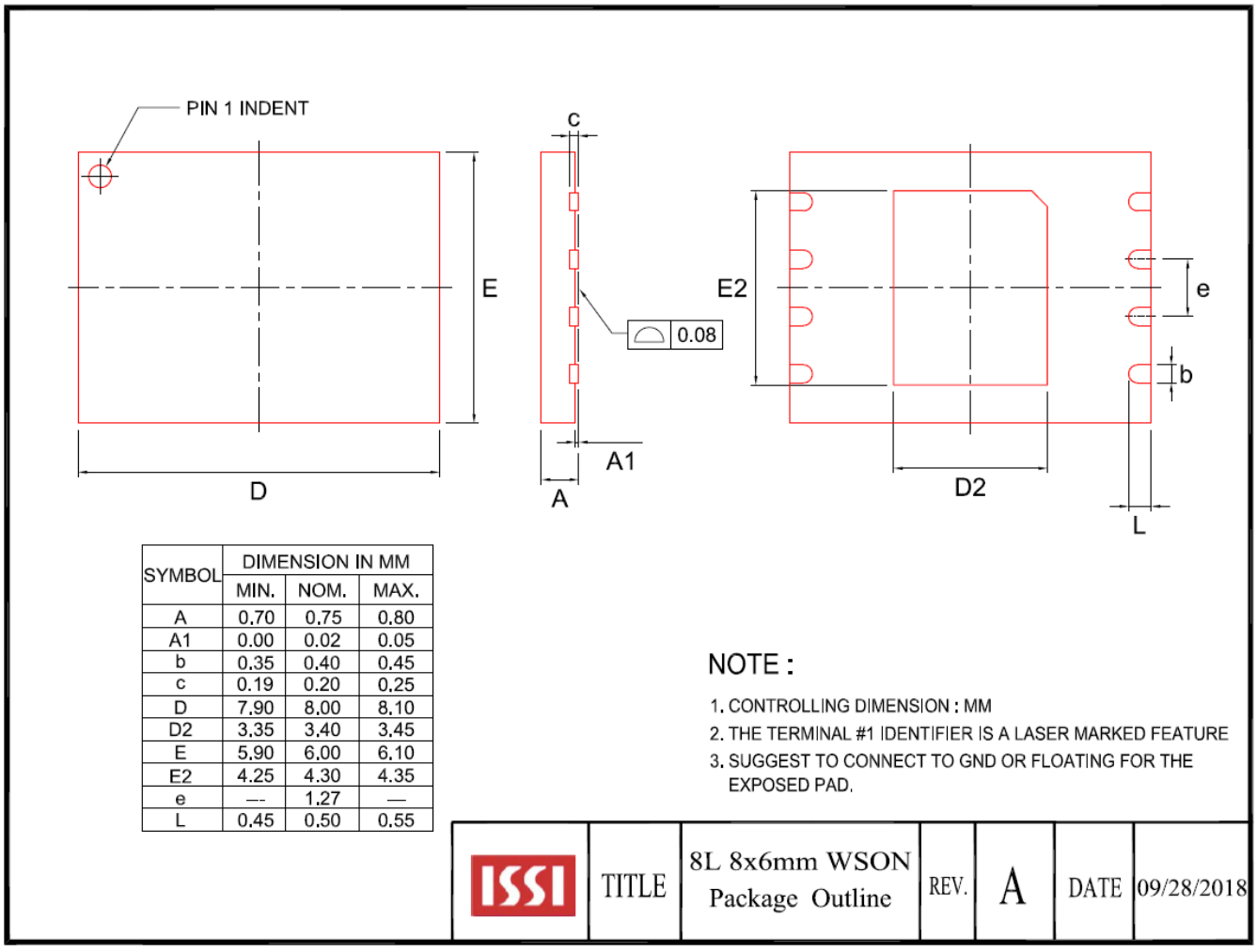
The failure of a page program operation does not affect the data in other pages in the same lock, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Table 8.6 Error Management Details

Operation	Description	Recommended procedure
Erase	Status register read after erase, check E_Fail bit	Block replacement
Program	Status register read after program, check P_Fail bit	Block replacement
Read	Status register read after read, check ECCS2, 1, 0 bit	ECC correction

9. PACKAGE INFORMATION

9.1 8- CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 8X6MM (J)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
c	0.19	0.20	0.25
D	7.90	8.00	8.10
D2	3.35	3.40	3.45
E	5.90	6.00	6.10
E2	4.25	4.30	4.35
e	---	1.27	---
L	0.45	0.50	0.55

NOTE :

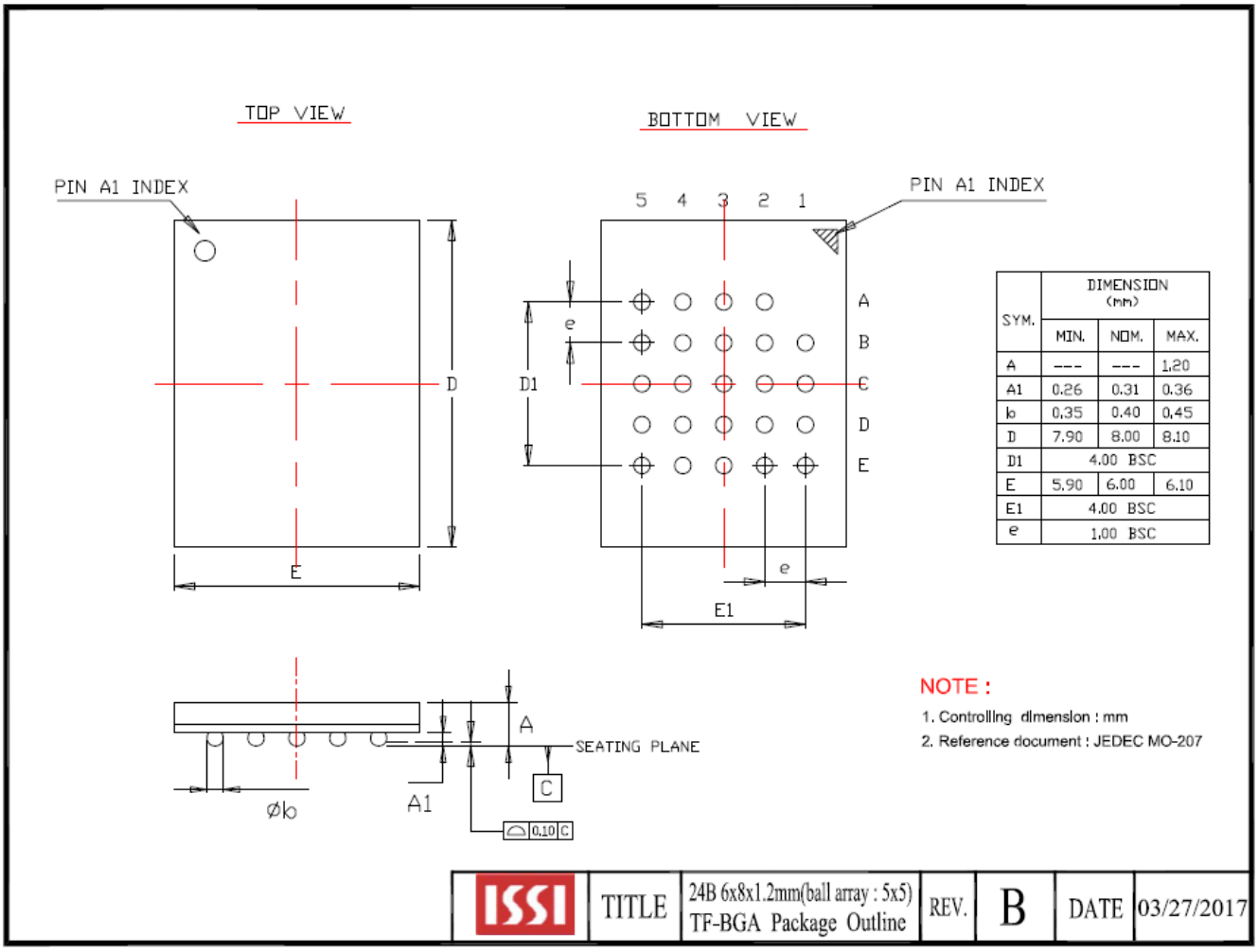
1. CONTROLLING DIMENSION : MM
2. THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE
3. SUGGEST TO CONNECT TO GND OR FLOATING FOR THE EXPOSED PAD.

	TITLE	8L 8x6mm WSON Package Outline	REV.	A	DATE	09/28/2018

Notes:

1. Please **click here** to refer to Application Note (AN25D011, Thin USON/WSON/XSON package handling precautions) for assembly guidelines.
2. **Pad Open size is 3.4mm x 4.3mm**

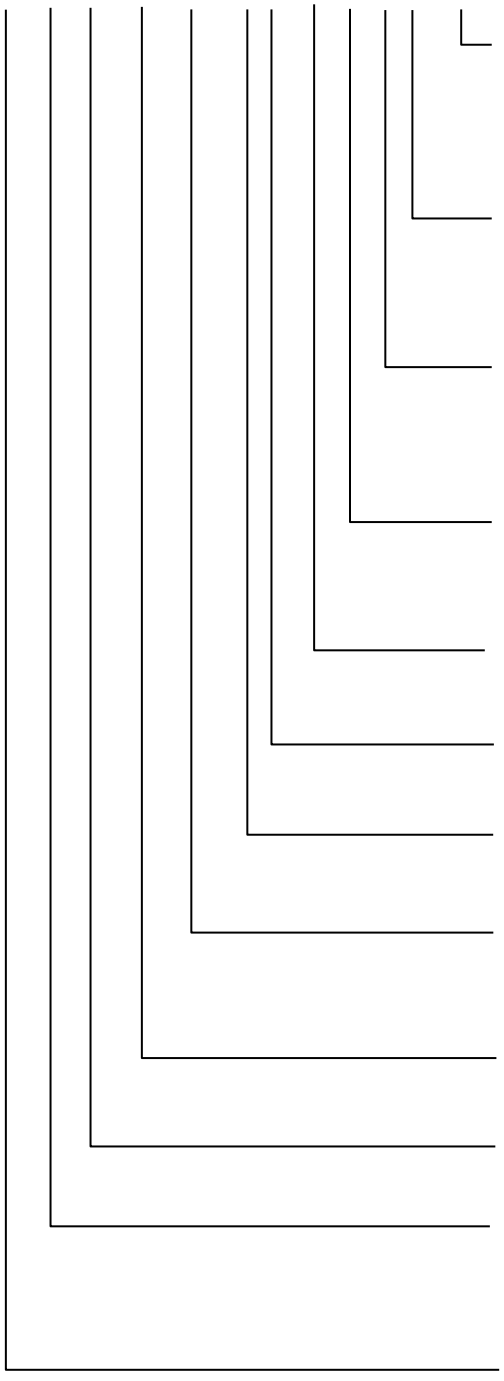
9.2 24-BALL THIN PROFILE FINE PITCH BGA 6X8X1.2MM 5X5 BALL ARRAY (H)



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

10. ORDERING INFORMATION – Valid Part Numbers

IS 37 SM L 02G 8 B - J H L I - TR



PACKING
TR = Tape and Reel
TY = Tray
Blank = Bulk

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT
L = Green Package **(**RoHS Compliant, Halogen-free) and TSCA Compliant

PACKAGE Type
J = 8-contact WSON (8x6mm), Pad Open = 3.4mmx4.3mm
H = 24-ball TFBGA 6x8x1.2 mm

Option
J = Normal

Die Revision
B = Gen. B

ECC Requirement
8 = 8-bit ECC

Density
01G = 1Gb
02G = 2Gb

VCC
L = 3.3V

Technology
SM = SPI-NAND (SLC)

Product Family
37 = SPI-NAND
38 = Automotive SPI-NAND

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.

Note:
1. Call Factory for other package options available.

VCC	Density	Temp. Grade	Order Part Number	Package
3.3V	1Gb	Industrial	IS37SML01G8B-JJLI	8-contact WSON 8x6mm
			IS37SML01G8B-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SML01G8B-JJLA2	8-contact WSON 8x6mm
			IS38SML01G8B-JHLA2	24-ball TFBGA 6x8x1.2 mm
	2Gb	Industrial	IS37SML02G8B-JJLI	8-contact WSON 8x6mm
			IS37SML02G8B-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SML02G8B-JJLA2	8-contact WSON 8x6mm
			IS38SML02G8B-JHLA2	24-ball TFBGA 6x8x1.2 mm

Note:

1. A1 meets AEC-Q100 requirements with PPAP.