IS25LX032 IS25WX032
IS25LX064 IS25WX064

64/32Mb

Serial Flash Memory Octal I/O
xSPI (eXpanded Serial Peripheral) Interface with On-CHIP ECC

166/(200)MHZ (1.8V), 133MHZ (3.0V)

DATA SHEET

64/32Mb SERIAL FLASH MEMORY Octal I/O xSPI (eXpanded SPI) with On Chip ECC 166(200)(5)MHz (1.8V), 133MHz (3.0V)

FEATURES

- **Industry Standard Serial Interface**
  - IS25LX064: 64Mbit/8Mbyte
  - IS25WX064: 64Mbit/8Mbyte
  - IS25LX032: 32Mbit/8Mbyte
  - IS25WX032: 32Mbit/8Mbyte
  - JEDEC Standard xSPI (eXpanded SPI) compliant
  - Protocol: Extended SPI (1S-xy-xy)(2)
    Octal DDR (8D-8D-8D)

- **High Performance**
  - Support clock frequency up to;
    - IS25WX (1.8V): SDR - 166MHz
      DDR – 166(200) (5) MHz
    - IS25LX (3.0V): SDR /DDR - 133MHz
  - Execute-in-place (XIP)
  - 2-bit Detection and 1-bit Correction per 16-byte boundary (with ECC)
  - Array Data CRC/ Address Parity function supported.
  - Optional PSC (Phase Shifted Clock) (1) is supported to put DQS on the center of read data valid window.
  - Data Learning Pattern for training operation
  - More than 100,000 Erase/Program Cycles
  - More than 20-year Data Retention

- **Security and Write Protection**
  - Volatile and nonvolatile locking and software write protection for each 128KB sector
  - Password Protection
  - Hardware write protection: nonvolatile bits (BP [3:0] and TB) define protected area size.

- **Efficient Read and Program modes**
  - Input Data Format
    SPI: 1-byte command+3/4 byte Address
    Octal: 2-byte command+4 byte Address
  - PROGRAM/ERASE SUSPEND operation
  - 128KB Sector Erase(3) and 4KB/32KB Subsector Erase

- **Low Power with Wide Temp. Ranges**
  - Single Voltage Supply
    IS25LX: 2.70V to 3.60V
    IS25WX: 1.70V to 2.0V
  - 6 µA Standby Current
  - 1 µA Deep Power Down
  - Temp Grades:
    Extended: -40°C to +105°C
    Auto A3 Grade: -40°C to +125°C

- **Flexible & Efficient Memory Architecture**
  - 4-Bank Architecture for READ While PROGRAM/ERASE Operations (4)
  - Program 1 to 256byte per Page
  - Dedicated 64-byte OTP area outside main memory

- **Hardware Features**
  - C Input : Serial Clock Input
  - DQ0 – DQ7: Serial Data Input and Output
  - RESET#: Hardware Reset pin
  - DQS: Data Strobe Signal
  - ERR#: Error Indication Signal
  - W#: Optional Write Protection Signal (1)

- **Electronic signature**
  - JEDEC –standard 3-byte signature
  - Extended device ID: two additional bytes identify device factory options

- **Configuration**
  - Boot in SDR x1
  - Boot in DDR x8 (Call Factory)

- **Industry Standard Pin-out & Packages**
  - H = 24-ball TFBGA 6x8mm (5x5 ball array)
  - KGD (Call Factory)
  - Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

Notes:
1. Dedicated W# and PSC clock are supported in optional devices only.
2. x= I/O width (x1 or x8), y= SDR or DDR
3. 64KB Sector Erase is supported as an option.
4. Read while Program/Erase function is supported with option L
5. Call Factory for 200MHz

GENERAL DESCRIPTION

The IS25LX064/032 and IS25WX064/032 Serial Flash memory offer a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is compliant with JEDEC Standard xSPI (eXpanded Serial Peripheral Interface).
Nonvolatile and volatile configuration registers enable respective default and temporary settings such as READ operation dummy cycles and wrap modes, memory protection, output buffer impedance, SPI protocol type, and XIP mode.
Memory is organized as uniform 128KB sectors, 4KB and 32KB subsectors, and 256 byte pages. Optional 64KB sectors are also supported.

The device includes 64-byte OTP area that can be permanently locked.

Direct boot in Octal DDR protocol provides high performance and ease of use, enabling communication between host and device without need to configure extended SPI protocol operations. However, the devices still support both extended SPI and Octal DDR protocols to ensure legacy system support and easy migration path. The extended SPI protocol supports address and data transmission on one or eight data lines, depending on the command.

XIP feature is supported in extended SPI because its commands are sent through DQ0 only.

Information in octal DDR protocol is always transmitted via eight data lines on both rising and falling clock edges. When accessing cell array (Read/Program), **minimum transferred data size is 2-bytes in DDR mode, so the LSB of starting address must be always "0".**

Most legacy x1 SPI commands are supported, but require only one clock cycle because command is latched on both rising and falling edges of the clock.

Address cycles are fixed at 4-byte (32-bit) operations from the flash array in octal DDR protocol.

The host does not need to drive DQS during the input operation to the memory. The data input (DQ) to the memory still relies on clock (C) to latch all address and data operations. Most register outputs require dummy clock cycles due to the critical timing from command decoding. With the help of DQS for output data latching, the number of dummy clock is transparent to the host.

Suspend and resume commands provide the ability to pause and resume PROGRAM/ERASE operations.

In an optional device (option L), Read while Write operation provides beginning of read operation from one of 3-banks while programming or erase operation is in progress at specific bank, without interruption of program or erase operation.

There are three type of data integrity check functions:
- ECC to prevent errors from stored data
- Address Parity check to prevent address transmission errors in Octal DDR mode only
- Array data CRC (Data Parity) to prevent data transmission errors in Octal DDR mode only.

Optional PSC (Phase Shifted Clock) is supported for Read operation only, to offset DQS signal, phase shifted from main clock (SCK) for controller to put DQS signal within valid data window in Octal DDR mode only.

Package, Voltage & Data Transfer Rate vs. Max. Frequency

Voltage	SDR	DDR
1.8V	166MHz	166(200) (1) MHz
3.0V	133MHz	133MHz

Note:
1. Call Factory for 200MHz

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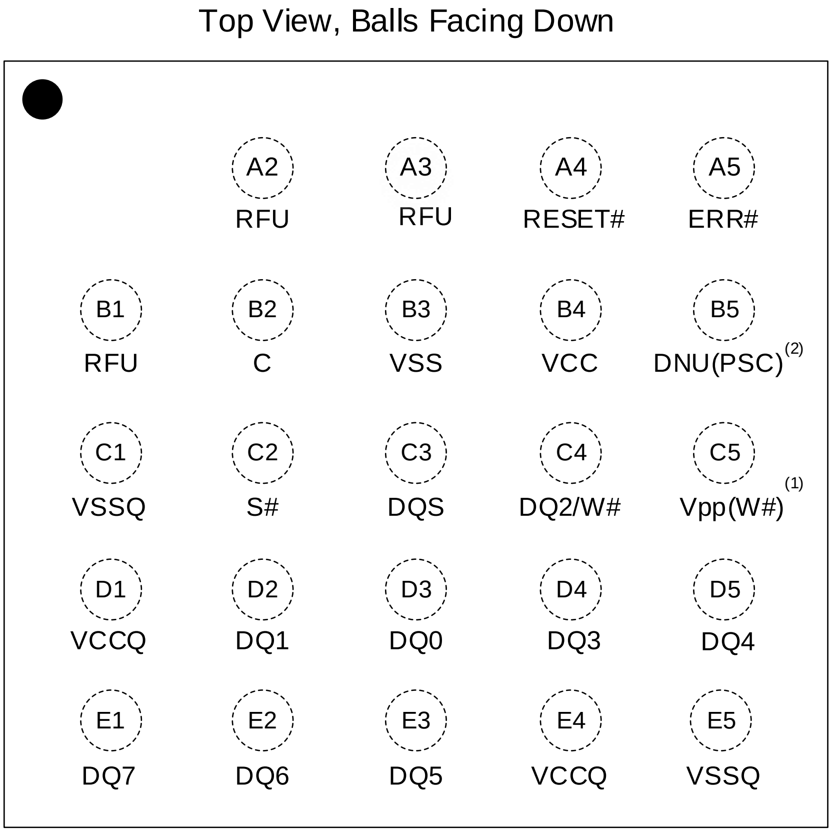
1. PIN CONFIGURATION

24-ball BGA (5x5 Array)



Notes:

1. **Dedicated W# instead of Vpp is supported as an optional device only. See the ordering information for detail.**
2. **Dedicated PSC (Phase Shifted Clock) is supported as an optional device only. See the ordering information for detail.**

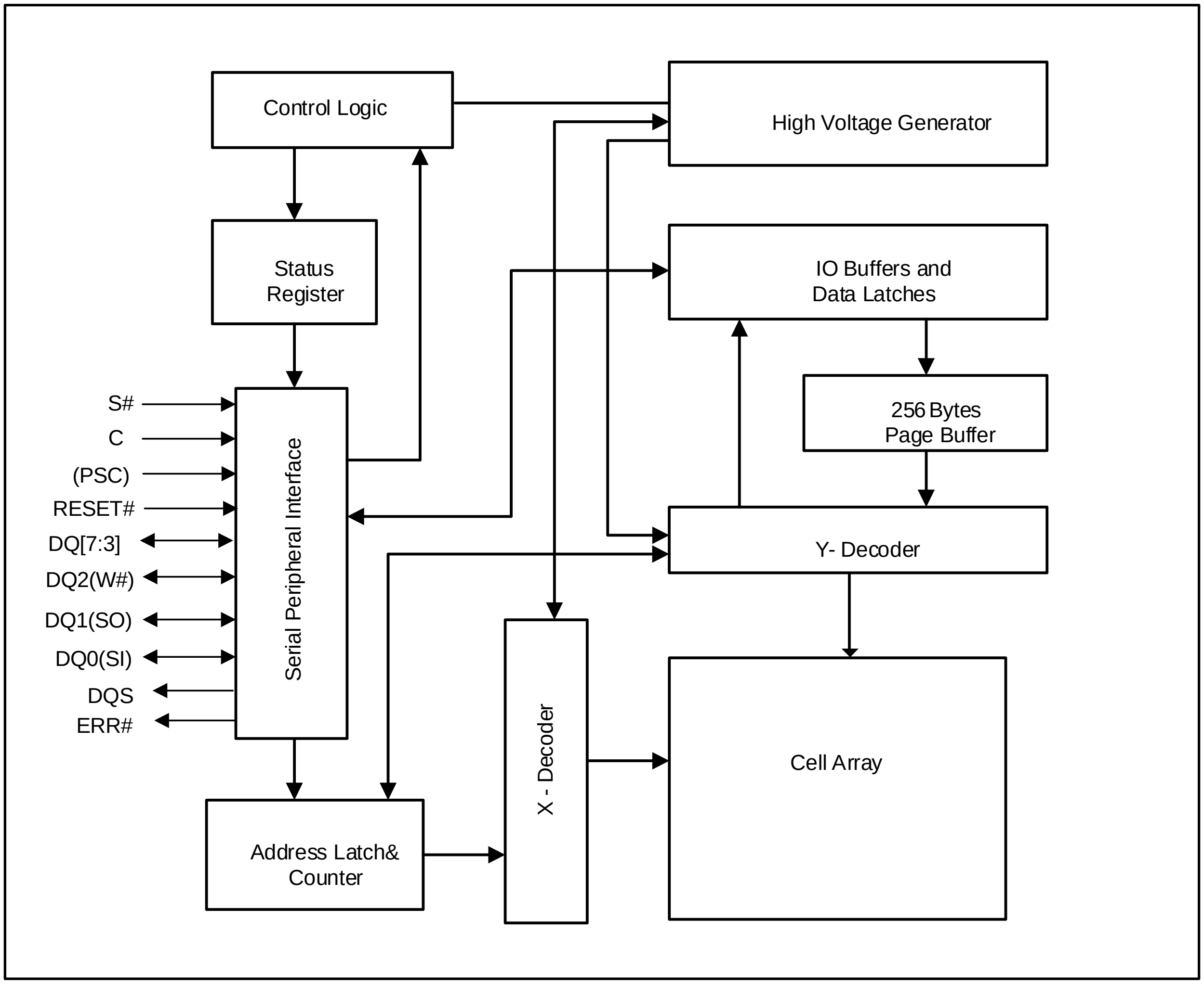
2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
C	INPUT	**Clock:** Provides timing for the serial interface. Command, address, or data inputs are latched on the rising edge of C. Data is shifted out on the falling edge of C.
S#	INPUT	**Chip Select:** The Chip select (S#) pin enables and disables the device operation.
RESET#	INPUT	**RESET#:** The RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. Internal Pull-Up.
W# (1)	INPUT	**Write Protect:** This input signal is used to freeze the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and W# signal is driven LOW, the status registor nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not be executed. During the extended-SPI protocol with OCTAL READ/PROGRAM instructions, and during octal DDR protocol, this pin functions an input/output (DQ2 functionality). But Dedicated W# ball instead of Vpp ball is available in BGA PKG (C5 ball) as an option. At that time, C4 ball will become DQ2 instead of DQ2/W#.
DQ[7:0]	INPUT/ OUTPUT	**Serial IO:** Bidirectional signals that transfer address, data, and command information. In extended-SPI protocol, DQ0 functions as an input for command. But address and data transfer on DQ [7:0] depends on the command. Input (address, write data) can be latched on the rising edge of C (SDR) or on both edges of C (DDR). Output data can be shifted out on the falling edge of C (SDR) or on both edges of C (DDR). In Octal DDR protocol, DQ[7:0] always function as I/O, input is latched on both edges of C, and output is shifted out on both edges of C.DQ2 is used also as write protection control.
DQS	OUTPUT	**Data Strobe Signal:** Indicates output data valid and is required to support high speed data output. Not necessary required in extended-SPI protocol except to achieve high frequency for specific DDR commands. Used for READ but not for WRITE operations. Configured by nonvolatile and volatile configuration register bit 5 at address 00h. When enabled, DQS is driven to ground at S# LOW and until the device is driving output data, in which case DQS toggles to synchronize data output. When not enabled, DQS is not driven.
ERR#	OUTPUT	**ECC Error Indication Signal:** Indicates ECC Event occurrence. Open Drain. External Pull-Up is required when using ERR# signal.
PSC (1)	INPUT	**Phase Shifted Clock:** Optional 2nd clock to offset DQS signal from main clock (C) PSC feature is available in Octal DDR mode only in BGA PKG as an option.
VCC, VCCQ	SUPPLY	**Supply voltage:** Core Power Supply (B4), I/O Power Supply (D1, E4)
Vpp	SUPPLY	**Supply voltage:** If Vpp is in the voltage of VPPH, the signal acts as an additional power supply for programming operation, as defined in the Operating Condition table. The Vpp pad will be internally pulled up to VCC, so customer can leave Vpp pin floated if not used.
VSS, VSSQ	GROUND	**Ground:** Core Ground (B3), I/O Ground (C1, E5).
RFU	-	**Reserved for future use:** Must be left floating.
DNU	-	**Do Not Use:** Must be left floating.

Note:

1. **Dedicated W# and PSC are supported in the optional device.**

3. BLOCK DIAGRAM



4. xSPI Signal Protocol Description

xSPI command protocol is for Octal DDR (x8) protocols and Extended SPI (x1) protocol.

- Octal DDR protocol
- Traditional Extended SPI protocol

Protocol	Command	Address	Remark
Octal DDR	2 byte, DDR (Valid byte + Repeated byte) (1) via DQ [7:0]	4-byte only	Command is valid byte and command extension is repeated byte.
Extended SPI	1 byte, SDR (Valid byte) via DQ0 only	3 or 4 byte	Defaults 3 byte address mode

Note:

1. **The device actually decodes 1st byte of valid byte on the rising edge of clock only in command, so repeated byte of command extension becomes dummy byte.**

ISSI xSPI device supports below operation:

- Extended SPI mode : 1S-xy-xy operation (x=bit width, y=SDR or DDR)
    - Command is always sent through DQ0 bit (x1), command with 3-byte address is default.
    - 1S-1S-1S: Traditional SPI protocol
    - 1S-1S-8S: Fast Read Octal Output operation and Octal Input Page Program operation
    - 1S-1D-8D: DDR Fast Read Octal Output operation.
    - 1S-8S-8S: Fast Read Octal IO operation and Extended Octal IO Page Program operation.
    - 1S-8D-8D: DDR Fast Read Octal IO operation (exceptional command with 4-byte address only).

- Octal DDR mode : 8D-8D-8D operation, command with 4-byte address only
    - Eight IO signals are used during command transfer, address transfer, and data transfer. . All phases are DDR.

Note: Minimum transferred data size is 2-bytes in DDR data transfer operation, so the LSB of starting address must be always "0".(1S-1D-8D, 1S-8D-8D, 8D-8D-8D)

In 1S-1S-1S mode, bit transfer uses DQ [0] to transfer information from master to slave and DQ [1] to transfer information from slave to master. On each IO, information is placed on the IO line in Most Significant Bit (MSB) to Least Significant Bit (LSB) order within each byte. Sequential command modifier bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.

Table 4.1 1S-1S-1S Bit Positions

DQ	Command Bits	Command Modifier Bits (address) (1)	Latency	Data Byte 0	Data Byte 1
0	7, 6, 5, 4, 3, 2, 1, 0	31 (23), 30 (22), … 1, 0	X …	X …	X …
1	X …	X …	X …	7, 6, 5, 4, 3, 2, 1, 0	7, 6, 5, 4, 3, 2, 1, 0
2	X …	X …	X …	X …	X …
3	X …	X …	X …	X …	X …
4	X …	X …	X …	X …	X …
5	X …	X …	X …	X …	X …
6	X …	X …	X …	X …	X …
7	X …	X …	X …	X …	X …

Note:

1. **3-byte or 4-byte address is followed.**

In 8D-8D-8D mode, bit transfer uses eight DQ signals of DQ [7:0]. The LSB of each byte is placed on DQ [0] with each higher order bit on the successively higher numbered DQ signals. Command is composed of valid command byte of bits [7:0]. Command Modifier Bits are composed of command extension byte (repeated byte) and address bytes (4-byte). All transfer is in DDR mode. **Minimum size of transferred Read/Write data is 2 byte (1 word) in DDR mode.**

Table 4.2 8D-8D-8D Bit Positions

DQ	Command Bits	Command Modifier Bits (command ext. & address)					Latency	Data Word 0		Data Word 1	
0	0	0	24	16	…	0	X …	0	0	0	0
1	1	1	25	17	…	1	X …	1	1	1	1
2	2	2	26	18	…	2	X …	2	2	2	2
3	3	3	27	19	…	3	X …	3	3	3	3
4	4	4	28	20	…	4	X …	4	4	4	4
5	5	5	29	21	…	5	X …	5	5	5	5
6	6	6	30	22	…	6	X …	6	6	6	6
7	7	7	31	23	…	7	X …	7	7	7	7

5. SYSTEM CONFIGURATION

The device is divided into uniform 128KB sector (or optional 64KB sector), and each sector is divided into 4KB/32KB subsectors.

In an optional device (option L), the memory array is divided into 4 Banks. The multi bank structure enables Read while Write operation, which means read cell array data from one bank while another bank is in the middle of program/erase operation.

The Status Register controls how the memory is protected.

5.1 BANK/BLOCK/SECTOR ADDRESSES

Table 5.1 Sector/Subsector Addresses (Sector Size = 128KB)

Memory Density		Sector No. (128Kbyte)	Subsector No. (32Kbyte)	Subsector No. (4Kbyte)	Address Range
32Mb	64Mb	Sector 0	Subsector 0	Subsector 0	000000h - 000FFFh
				:	:
			Subsector 1	:	:
				Subsector 15	00F000h - 00FFFFh
			Subsector 2	Subsector 16	010000h - 010FFFh
				:	:
			Subsector 3	:	:
				Subsector 31	01F000h - 01FFFFh
		:	:	:	:
		Sector 31	Subsector 124	Subsector 992	3E0000h – 3E0FFFh
				:	:
			Subsector 125	:	:
				Subsector 1007	3EF000h – 3EFFFFh
			Subsector 126	Subsector 1008	3F0000h – 3F0FFFh
				:	:
			Subsector 127	:	:
				Subsector 1023	3FF000h – 3FFFFFh
		:	:	:	:
		Sector 63	Subsector 252	Subsector 2016	7E0000h – 7E0FFFh
				:	:
			Subsector 253	:	:
				Subsector 2031	7EF000h – 7EFFFFh
			Subsector 254	Subsector 2032	7F0000h – 7F0FFFh
				:	:
			Subsector 255	:	:
				Subsector 2047	7FF000h – 7FFFFFh

Note:

1. Below is the mapping for bank & Sector when Sector size is 128KB in an optional device (option L)

	Bank 0	Bank 1	Bank 2	Bank 3	Remark
64Mb	Sector 0~15	Sector 16~31	Sector 32~47	Sector 48~63	
32Mb	Sector 0~7	Sector 8~15	Sector 16~23	Sector 24~31	

Table 5.2 Table Sector/Subsector Addresses (Sector Size = 64KB)

Memory Density		Sector No. (64Kbyte)	Subsector No. (32Kbyte)	Subsector No. (4Kbyte)	Address Range
32Mb	64Mb	Sector 0	Subsector 0	Subsector 0	000000h - 000FFFh
				:	:
			Subsector 1	:	:
				Subsector 15	00F000h - 00FFFFh
		Sector 1	Subsector 2	Subsector 16	010000h - 010FFFh
				:	:
			Subsector 3	:	:
				Subsector 31	01F000h - 01FFFFh
		:	:	:	:
		Sector 62	Subsector 124	Subsector 992	3E0000h – 3E0FFFh
				:	:
			Subsector 125	:	:
				Subsector 1007	3EF000h – 3EFFFFh
		Sector 63	Subsector 126	Subsector 1008	3F0000h – 3F0FFFh
				:	:
			Subsector 127	:	:
				Subsector 1023	3FF000h – 3FFFFFh
		:	:	:	:
		Sector 126	Subsector 252	Subsector 2016	7E0000h – 7E0FFFh
				:	:
			Subsector 253	:	:
				Subsector 2031	7EF000h – 7EFFFFh
		Sector 127	Subsector 254	Subsector 2032	7F0000h – 7F0FFFh
				:	:
			Subsector 255	:	:
				Subsector 2047	7FF000h – 7FFFFFh

Note:

1. Below is the mapping for bank & Sector when Sector size is 64KB in an optional device (option L)

	Bank 0	Bank 1	Bank 2	Bank 3	Remark
64Mb	Sector 0~31	Sector 32~63	Sector 64~95	Sector 96~127	
32Mb	Sector 0~15	Sector 16~31	Sector 32~47	Sector 48~63	

5.2 SERIAL FLASH DISCOVERABLE PARAMETERS

The Serial Flash Discoverable Parameters (SFDP) standard defines the structure of the SFDP database within the memory device. SFDP is the standard of JEDEC JESD216.

The JEDEC-defined header with Parameter ID FF00h and related Basic Parameter Table is mandatory. Additional parameter headers and tables are optional.

6. REGISTERS

6.1 STATUS REGISTER

Status register bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively. When the status register enable /disable bit (bit 7) is set to 1 and W# is driven LOW, the status register nonvolatile bits become read only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to driven W# HIGH.

Table 6.1 Status Register Bit Definition

Bit	Name	Settings	Definition	Notes
7	SRWD	0 = Enabled (default) 1 = Disabled	**Nonvolatile control bit:** Used with W# to enable or disable writing to the status register:	-
5	TB	0 = Top (default) 1 = Bottom	**Nonvolatile control bit**: Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	-
6, 4:2	BP[3:0]	See Protected Area tables	**Nonvolatile control bit**: Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations. All bits = 0 (default)	1
1	WEL	0 = Clear (default) 1 = Set	**Volatile control bit**: The device always powers up with this bit cleared to prevent inadvertent WRITE, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to see this bit.	-
0	WIP	0 = Ready(default) 1 = Busy	**Volatile status bit**: Indicates if one of the following command cycles in in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	2

Notes:
1. The CHIP ERASE command is executed only if all bits = 0.
2. Status register bit 0 is the inverse of flag status register bit 7.

Table 6.2 Block assignment by Block Protect (BP) Bits

Status Register Bits				Byte Protected	Protected Memory Area for 64Mb (Block Size = 128KB), 64 blocks	
BP3	BP2	BP1	BP0		TBS = 0, Top area	TBS = 1, Bottom area
0	0	0	0	0KB	0 (None)	0 (None)
0	0	0	1	128KB	1 (1 block : 63rd)	1 (1 block : 0th)
0	0	1	0	256KB	2 (2 blocks : 62nd and 63rd)	2 (2 blocks : 0th and 1st)
0	0	1	1	512KB	3 (4 blocks : 60th to 63rd)	3 (4 blocks : 0th to 3rd)
0	1	0	0	1MB	4 (8 blocks : 56th to 63rd)	4 (8 blocks : 0th to 7th)
0	1	0	1	2MB	5 (16 blocks : 48th to 63rd)	5 (16 blocks : 0th to 15th)
0	1	1	0	4MB	6 (32 blocks : 32nd to 63rd)	6 (32 blocks : 0th to 31st)
0	1	1	1	8MB	7 (64 blocks : 0th to 63rd)	7 (64 blocks : 0th to 63rd)
1	0	0	0	8MB	8 (64 blocks : 0th to 63rd)	8 (64 blocks : 0th to 63rd)
1	0	0	1	5MB (All)	9 (40 blocks : 24th to 63rd)	12 (40 blocks : 0th to 39th)
1	0	1	0	6MB (All)	10 (48 blocks : 16th to 63rd)	13 (48 blocks : 0th to 47th)
1	0	1	1	7MB (All)	11 (56 blocks : 8th to 63rd)	14 (56 blocks : 0th to 55th)
1	1	0	0	7680KB (All)	12 (60 blocks : 4th to 63rd)	12 (60 blocks : 0th to 59th)
1	1	0	1	7936KB (All)	13 (62 blocks : 2nd to 63rd)	13 (62 blocks : 0th to 61st)
1	1	1	0	8064KB (All)	14 (63 blocks : 1st to 63rd)	14 (63 blocks : 0th to 62nd)
1	1	1	1	8MB (All)	15 (64 blocks : 0th to 63rd)	15 (64 blocks : 0th to 63rd)

Status Register Bits				Byte Protected	Protected Memory Area for 32Mb (Block Size = 128KB), 32 blocks	
BP3	BP2	BP1	BP0		TBS = 0, Top area	TBS = 1, Bottom area
0	0	0	0	0KB	0 (None)	0 (None)
0	0	0	1	128KB	1 (1 block : 31st)	1 (1 block : 0th)
0	0	1	0	256KB	2 (2 blocks : 30th and 31st)	2 (2 blocks : 0th and 1st)
0	0	1	1	512KB	3 (4 blocks : 28th to 31st)	3 (4 blocks : 0th to 3rd)
0	1	0	0	1MB	4 (8 blocks : 24th to 31st)	4 (8 blocks : 0th to 7th)
0	1	0	1	2MB	5 (16 blocks : 16th to 31st)	5 (16 blocks : 0th to 15th)
0	1	1	0	4MB	6 (32 blocks : 0th to 31st)	6 (32 blocks : 0th to 31st)
0	1	1	1	4MB	7 (32 blocks : 0th to 31st)	7 (32 blocks : 0th to 31st)
1	0	0	0	4MB	8 (32 blocks : 0th to 31st)	8 (32 blocks : 0th to 31st)
1	0	0	1	2.5MB (All)	9 (20 blocks : 12th to 31st)	12 (20 blocks : 0th to 19th)
1	0	1	0	3MB (All)	10 (24 blocks : 8th to 31st)	13 (24 blocks : 0th to 23rd)
1	0	1	1	3.5MB (All)	11 (28 blocks : 4th to 31st)	14 (28 blocks : 0th to 27th)
1	1	0	0	3840KB (All)	12 (30 blocks : 2nd to 31st)	12 (30 blocks : 0th to 29h)
1	1	0	1	3968KB (All)	13 (31 blocks : 1st to 31st)	13 (31 blocks : 0th to 30th)
1	1	1	0	4MB (All)	14 (32 blocks : 0th to 31st)	14 (32 blocks : 0th to 31st)
1	1	1	1	4MB (All)	15 (32 blocks : 0th to 31st)	15 (32 blocks : 0th to 31st)

Table 6.3 Block assignment by Block Protect (BP) Bits for Optional 64KB Sector Size

Status Register Bits				Byte Protected	Protected Memory Area for 64Mb (Block Size = 64KB), 128 blocks	
BP3	BP2	BP1	BP0		TBS = 0, Top area	TBS = 1, Bottom area
0	0	0	0	0KB	0 (None)	0 (None)
0	0	0	1	64KB	1 (1 block : 127th)	1 (1 block : 0th)
0	0	1	0	128KB	2 (2 blocks : 126th and 127th)	2 (2 blocks : 0th and 1st)
0	0	1	1	256KB	3 (4 blocks : 124th to 127th)	3 (4 blocks : 0th to 3rd)
0	1	0	0	512KB	4 (8 blocks : 120th to 127th)	4 (8 blocks : 0th to 7th)
0	1	0	1	1MB	5 (16 blocks : 112nd to 127th)	5 (16 blocks : 0th to 15th)
0	1	1	0	2MB	6 (32 blocks : 96th to 127th)	6 (32 blocks : 0th to 31st)
0	1	1	1	4MB	7 (64 blocks : 64th to 127th)	7 (64 blocks : 0th to 63rd)
1	0	0	0	6MB	8 (96 blocks : 32nd to 127th)	8 (96 blocks : 0th to 95th)
1	0	0	1	7MB	9 (112 blocks : 16th to 127th)	9 (112 blocks : 0th to 111st)
1	0	1	0	7680KB	10 (120 blocks : 8th to 127th)	10 (120 blocks : 0th to 119th)
1	0	1	1	7936KB	11 (124 blocks : 4th to 127th)	11 (124 blocks : 0th to 123rd)
1	1	0	0	8064KB	12 (126 blocks : 2nd to 127th)	12 (126 blocks : 0th to 125th)
1	1	0	1	8128KB	13 (127 blocks : 1st to 127th)	13 (127 blocks : 0th to 126th)
1	1	1	0	8MB (All)	14 (128 blocks : 0th to 127th)	14 (128 blocks : 0th to 127th)
1	1	1	1	8MB (All)	15 (128 blocks : 0th to 127th)	15 (128 blocks : 0th to 127th)

Status Register Bits				Byte Protected	Protected Memory Area for 32Mb (Block Size = 64KB), 64 blocks	
BP3	BP2	BP1	BP0		TBS = 0, Top area	TBS = 1, Bottom area
0	0	0	0	0KB	0 (None)	0 (None)
0	0	0	1	64KB	1 (1 block : 63rd)	1 (1 block : 0th)
0	0	1	0	128KB	2 (2 blocks : 62nd and 63rd)	2 (2 blocks : 0th and 1st)
0	0	1	1	256KB	3 (4 blocks : 60th to 63rd)	3 (4 blocks : 0th to 3rd)
0	1	0	0	512KB	4 (8 blocks : 56th to 63rd)	4 (8 blocks : 0th to 7th)
0	1	0	1	1MB	5 (16 blocks : 48th to 63rd)	5 (16 blocks : 0th to 15th)
0	1	1	0	2MB	6 (32 blocks : 32nd to 63rd)	6 (32 blocks : 0th to 31st)
0	1	1	1	3MB	7 (48 blocks : 16th to 63rd)	10 (48 blocks :0th to 47th)
1	0	0	0	3.5MB	8 (56 blocks : 8th to 63rd)	11 (56 blocks : 0th to 55th)
1	0	0	1	3840KB	9 (60 blocks : 4th to 63rd)	12 (60 blocks : 0th to 59th)
1	0	1	0	3968KB	10 (62 blocks : 2nd to 63rd)	13 (62 blocks : 0th to 61st)
1	0	1	1	4032KB	11 (63 blocks : 1st to 63rd)	14 (63 blocks : 0th to 62nd)
1	1	0	0	4MB (All)	12 (64 blocks : 0th to 63rd)	12 (64 blocks : 0th to 63rd)
1	1	0	1	4MB (All)	13 (64 blocks : 0th to 63rd)	13 (64 blocks : 0th to 63rd)
1	1	1	0	4MB (All)	14 (64 blocks : 0th to 63rd)	14 (64 blocks : 0th to 63rd)
1	1	1	1	4MB (All)	15 (64 blocks : 0th to 63rd)	15 (64 blocks : 0th to 63rd)

6.2 FLAG STATUS REGISTER

Flag status register bits are read by using READ FLAG STATUS REGISTER command. All bits are volatile and are reset to zero on power up.

Status bits are set and reset automatically by the internal controller. Error bits must be cleared through the CLEAR STATUS REGISTER command.

Table 6.4 Flag Status Register

Bit	Name	Settings	Definition
7	Program or erase controller	0 = Busy 1 = Ready	**Status bit:** Indicates whether one of the following operation is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE
6	Erase suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.
5	Erase	0 = Clear 1 = Failure or protection error	**Error bit**: Indicates whether an ERASE operation has succeeded or failed.
4	Program	0 = Clear 1 = Failure or protection error	**Error bit**: Indicates whether a PROGRAM operation has succeeded or failed.
3	Reserved	0	Reserved
2	Program suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.
1	Protection	0 = Clear 1 = Failure or protection error	**Error bit**: Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	**Status bit**: Indicates whether 3-byte or 4-byte address mode is enabled.

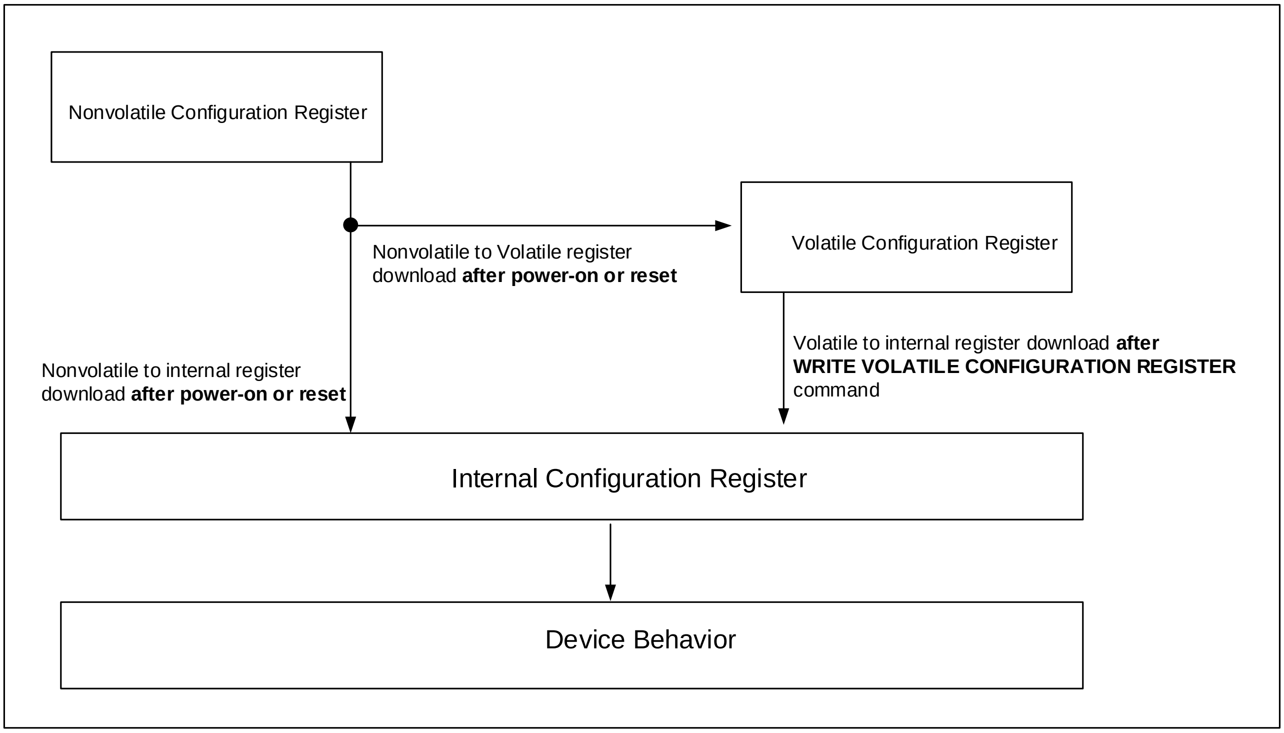
6.3 INTERNAL CONFIGURATION REGISTER

The memory configuration is set by an internal configuration register that is not directly accessible to users.

The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.

The user can change the configuration during device operation using the WRITE VOLATILE CONFIGURATION REGISTER command. Information from the volatile configuration register overwrites the internal configuration register immediately after the WRITE command completes.

Figure 6.1 Internal Configuration Register



6.4 NONVOLATILE CONFIGURATION REGISTER

Nonvolatile configuration register bits set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and WRITE NONVOLATILE CONFIGURATION REGISTER command, respectively. The commands use the main array address scheme, but only the LSB is used to access different register settings, thereby providing up to 256 bytes of registers. A READ command from reserved address returns FFh. A WRITE command to a reserved setting is ignored, flag status register bit 1 is set, and the write enable latch bit is cleared.

Table 6.5 Nonvolatile Configuration Register

Address	Bit	Name	Settings	Description	Notes
FFh:0Ch		Reserved	Reserved	Reserved	
0Bh	[7]	RCRCENB	1 = CRC Disabled (Default) 0 = CRC Enabled	Address Parity and Array Read Data Parity Enabled or Disabled in Octal DDR Read operation.	
	[6]	SSOENB	1 = All 8 DQs are same (Default) 0 = DQ3 is inverted, and remaining IOs are same.	SSO pattern of DLP Enabled or Disabled. SSO pattern means IO3 is inverted and other 7 IOs are the same.	
	[5:4]	CRCSIZE	11 = 16-byte (Default) 10 = 32-byte 01 = 64-byte 00 = 128-byte	Selects chunk size for Program CRC operation.	
	[3]	WCRCENB	1 = CRC Disabled (Default) 0 = CRC Enabled	Address Parity and Array Program Data Parity Enabled or Disabled in Octal DDR Program operation.	
	[2]	ERRBECC	1 = ERR# indicates 2–bit detection.(Default) 0 = ERR# LOW indicates 1-bt correction.	ERR# LOW behavior for 1-bit correction or 2-bit detection out of ECC event. Also it will determine ECC error type for ECCFCA bits. Only valid when ECCENB bit is 0.	
	[1]	ERRBENB	1 = ERR# OFF (Default) 0 = ERR# ON	Enable or disable ERR# signal, which indicates ERR error.	
	[0]	ECCENB	1 = ECC OFF (Default) 0 = ECC ON	Enables or Disables ECC	
0Ah	[7:0]	DLP Pattern	55h = 01010101 (Default) Bit 7 is an MSB	Data Learning Pattern for training.	
09h:08h		Reserved	Reserved	Reserved	

Nonvolatile Configuration Register (Continued)

Address	Bit	Name	Settings	Description	Notes
07h	[7:0]	Wrap configuration	FFh = Continuous (Default) FEh = 64-byte wrap FDh = 32-byte wrap FCh = 16-byte wrap Others = Reserved	Enables the device to read from memory sequentially or to wrap within 16-, 32-, or 64-byte boundaries	
06h	[7:0]	XIP Configuration	FFh = XIP disabled (Default) FEh = 8IOFR XIP FDh = 8OFR XIP F8h = FAST READ XIP Others = Reserved		
05h	[7:0]	Beyond 128Mb address configuration	FFh = 3-byte address (Default) FEh = 4-byte address Others = Reserved	Defines the number of address bytes for a command.	
04h	[7:0]	Reserved	Reserved	Reserved	
03h	[7:0]	Programmable output drive strength	IS25LX: FFh = 50 ohm (Default) FEh = 35 ohm FDh = 25 ohm FCh = 18 ohm Others = Reserved IS25WX: FFh = 50 ohm (Default) FEh = 75 ohm FDh = 35 ohm FCh = 18 ohm Others = Reserved	Optimizes the impedance at VCC/2 output voltage.	
02h	[7:0]	Reserved	Reserved	Reserved	
01h	[7:0]	Dummy cycle configuration	00h = Identical to 1Fh 01h = 1 dummy cycle 02h = 2 dummy cycle 03h to 1Dh = 3 to 29 dummy cycles 1Eh = 30 dummy cycles 1Fh = Default Others = Reserved	Sets the number of dummy cycles subsequent to all FAST READ, OTP READ (4Bh), and DLP READ (CDh) commands (See the Command Set Table for default setting values).	1
00h	[7:0]	I/O mode	FFh = Extended SPI (Default) DFh = Extended SPI without DQS E7h = Octal DDR C7h = Octal DDR without DQS Others = Reserved	Sets the device to work in different I/O modes such as DDR mode or DQS mode (Strobe enabled)	2

Notes:

1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ, OTP READ, and DLP Read command (See Supported Clock Frequency Table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data. Dummy cycle for DLP READ = Dummy cycle setting of OCTAL DDR mode + 2 clock cycles. 18 clock cycle is a default setting.

2.For parts configured with pin configuration option "**Boot in DDR x8" the default value of this byte is FFh. On those parts it's not possible to configure the parts to work in extended SPI using NVCR. Only Octal DDR with DQS mode is supported.**

6.5 VOLATILE CONFIGURATION REGISTER

Volatile configuration register bits temporarily set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ VOLATILE CONFIGURATION REGISTER and WRITE VOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme, but only the LSB is used to access different register settings, thereby providing up to 256 bytes of registers. A READ command from reserved address returns FFh. A WRITE command to a reserved setting is ignored, flag status register bit 1 is set, and the write enable latch bit is cleared.

Table 6.6 Volatile Configuration Register

Address	Bit	Name	Settings	Description	Notes
FFh:12h		Reserved	Reserved	Reserved	
11h	[7:3]	Reserved	Reserved	Reserved	
	[2:0]	BANKSTAT (4)	000 = No Active program/erase operation 100 = program/erase operation in bank 0 101 = program/erase operation in bank 1 110 = program/erase operation in bank 2 111 = program/erase operation in bank 3	Indicates Active program/erase operation at specific bank. Useful for read while program/erase operation.	
10h	[7:0]	ECCFCA	Chunk address, [AA31:A24]	1st ECC Event occurred chunk address ; 1-bit correction event or 2-bit detection event will be depends on setting of ERRBECC bit (bit 2 of address 0Bh)	
0Fh	[7:0]	ECCFCA	Chunk address, [A23:A16]		
0Eh	[7:0]	ECCFCA	Chunk address, [A15:A8]		
0Dh	[7:4]	ECCFCA	Chunk address, [A7:A4]		
	[3:0]	Reserved	Reserved (outputs 0000)	Reserved	
0Ch	[7]	IPA_ECCB	0 = NO double programming or partial programming attempt within ECC chunk without erase (default) 1 = Yes double programming or partial programming attempt within ECC chunk without erase.	Indicates if there is an attempt for Incremental (Double) Programming within ECC boundary. Incremental programming is not allowed within ECC boundary when ECC is ON.	
	[6:3]	ECCCOUNTER	0000 = NO ECC event (default) 0001 = 1 ECC event 1111 = 15 ECC events	Store cumulative ECC event occurrence. Max. 15 ECC event occurrence can be stored, and stays 15 after further occurrence.	2
	[2]	ECCSTAT	0 = No error (default) 1 = 2-bit Error Detection	Indicates any 2-bit Error detection	
	[1]	PARSTAT	0 = No error (default) 1= Address Parity Error	Indicates any Address Parity Error detection	
	[0]	CRCSTAT	0 = No error (default) 1= Array Data CRC Error	Indicates any Array Data CRC Error detection or chunk address boundary violation detection.	

Table 6.6 Volatile Configuration Register (Continued)

Address	Bit	Name	Settings	Description	Notes
0Bh	[7]	RCRCENB	1 = CRC Disabled (Default) 0 = CRC Enabled	Address Parity and Array Read Data Parity Enabled or Disabled in Octal DDR Read operation.	
	[6]	SSOENB	1 = All 8 DQs are same (Default) 0 = DQ3 is inverted, and remaining IOs are same.	SSO pattern of DLP Enabled or Disabled. SSO pattern means IO3 is inverted and other 7 IOs are the same.	
	[5:4]	CRCSIZE	11 = 16-byte (Default) 10 = 32-byte 01 = 64-byte 00 = 128-byte	Selects chunk size for Program CRC operation.	
	[3]	WCRCENB	1 = CRC Disabled (Default) 0 = CRC Enabled	Address Parity and Array Program Data Parity Enabled or Disabled in Octal DDR Program operation.	
	[2]	ERRBECC	1 = ERR# indicates 2–bit detection.(Default) 0 = ERR# LOW indicates 1-bt correction.	ERR# LOW behavior for 1-bit correction or 2-bit detection out of ECC event. Also it will determine ECC error type for ECCFCA bits. Only valid when ECCENB bit is 0.	
	[1]	ERRBENB	1 = ERR# OFF (Default) 0 = ERR# ON	Enable or disable ERR# signal, which indicates ERR error	
	[0]	ECCENB	1 = ECC OFF (Default) 0 = ECC ON	Enables or Disables ECC	
0Ah	[7:0]	DLP Pattern	55h = 01010101 (Default), Bit 7 is an MSB	Data Learning Pattern for training.	
09h:08h		Reserved	Reserved	Reserved	

Table 6.6 Volatile Configuration Register (Continuted)

Address	Bit	Name	Settings	Description	Notes
07h	[7:0]	Wrap configuration	FFh = Continuous (Default) FEh = 64-byte wrap FDh = 32-byte wrap FCh = 16-byte wrap Others = Reserved	Enables the device to read from memory sequentially or to wrap within 16-, 32-, or 64-byte boundaries	
06h	[7:0]	XIP Configuration	FFh = XIP disabled (Default) FEh = XIP enabled Others = Reserved	Enables the device to operate in the selected XIP mode. It is first required to enable XIP and then enter XIP mode using the XIP confirmation bit.	
05h	[7:0]	Beyond 128Mb address configuration	FFh = 3-byte address (Default) FEh = 4-byte address Others = Reserved	Defines the number of address bytes for a command.	
04h	[7:0]	Reserved	Reserved	Reserved	
03h	[7:0]	Programmable output drive strength	IS25LX: FFh = 50 ohm (Default) FEh = 35 ohm FDh = 25 ohm FCh = 18 ohm Others = Reserved IS25WX: FFh = 50 ohm (Default) FEh = 75 ohm FDh = 35 ohm FCh = 18 ohm Others = Reserved	Optimizes the impedance at VCC/2 output voltage.	
02h	[7:0]	Reserved	Reserved	Reserved	
01h	[7:0]	Dummy cycle configuration	00h = Identical to 1Fh 01h = 1 dummy cycle 02h = 2 dummy cycle 03h to 1Dh = 3 to 29 dummy cycles 1Eh = 30 dummy cycles 1Fh = Default Others = Reserved	Sets the number of dummy cycles subsequent to all FAST READ, OTP READ (4Bh), and DLP READ (CDh) commands (See the Command Set Table for default setting values).	1
00h	[7:0]	I/O mode	FFh = Extended SPI (Default) DFh = Extended SPI without DQS E7h = Octal DDR C7h = Octal DDR without DQS Others = Reserved	Sets the device to work in different I/O modes such as DDR mode or DQS mode (Strobe enabled)	3

Note:

1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ, OTP READ, and DLP Read command (See Supported Clock Frequency Table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data. Dummy cycle for DLP READ = Dummy cycle setting of OCTAL DDR mode + 2 clock cycles. 18 clock cycle is a default setting.
2. ECC event counter (bit [6:3] of address 0Ch) stops counting once reach maximum value 15.
3. For parts configured with pin configuration option "**Boot in DDR x8" the default value of this byte is FFh. On those parts it's not possible to configure the parts to work in extended SPI using VCR. Only Octal DDR with DQS mode is supported.**
4. BANKSTAT bits are supported in an optional device only (option L).

Table 6.7 Maximum Clock Frequencies – SDR and DDR Read Starting at Any Byte Address

IS25WX(VCC = 1.7V to 2.0V, DDR=166MHz)

Number of Dummy Clock Cycles	Fast Read	Octal Output Fast Read		Octal I/O Fast Read		Octal DDR (8D-8D-8D)
	SDR (1S-1S-1S)	SDR (1S-1S-8S)	DDR (1S-1D-8D)	SDR (1S-8S-8S)	DDR (1S-8D-8D)	
1	67	16	NA	NA	NA	NA
2	85	33	16	NA	NA	NA
3	101	50	33	16	16	16
4	118	66	50	33	33	33
5	135	83	66	50	40	40
6	156	100	83	66	50	50
7	166	120	95	76	66	66
8		130	105	86	83	83
9		140	114	95	95	95
10		150	124	105	105	105
11		160	133	114	114	114
12		166	143	124	124	124
13			152	133	133	133
14			166	143	143	143
15				152	152	152
16				162	162	162
17				166	166	166
18						
19						
20 and above						

Note:
1. Values are guaranteed by characterization and not 100% tested in production

IS25WX(VCC = 1.7V to 2.0V, DDR=200MHz) (2)

Number of Dummy Clock Cycles	Fast Read	Octal Output Fast Read		Octal I/O Fast Read		Octal DDR (8D-8D-8D)
	SDR (1S-1S-1S)	SDR (1S-1S-8S)	DDR (1S-1D-8D)	SDR (1S-8S-8S)	DDR (1S-8D-8D)	
1	67	16	NA	NA	NA	NA
2	85	33	16	NA	NA	NA
3	101	50	33	16	16	16
4	118	66	50	33	33	33
5	135	83	66	50	50	50
6	156	100	83	66	66	66
7	166	120	95	76	76	76
8		130	114	86	86	86
9		140	124	95	95	95
10		150	133	105	105	105
11		160	143	114	114	114
12		166	152	124	124	124
13			162	133	133	133
14			171	143	143	143
15			181	152	152	152
16			191	162	162	162
17			200	166	171	171
18					181	181
19					191	191
20 and above					200	200

Notes:
1. Values are guaranteed by characterization and not 100% tested in production
2. Call Factory for 200MHz

IS25LX (VCC = 2.7V to 3.6V, DDR=133MHz)

Number of Dummy Clock Cycles	Fast Read	Octal Output Fast Read		Octal I/O Fast Read		Octal DDR (8D-8D-8D)
	SDR (1S-1S-1S)	SDR (1S-1S-8S)	DDR (1S-1D-8D)	SDR (1S-8S-8S)	DDR (1S-8D-8D)	
1	67	16	NA	NA	NA	NA
2	85	33	16	NA	NA	NA
3	101	50	33	16	16	16
4	118	66	50	33	33	33
5	133	83	66	50	50	50
6		100	83	66	66	66
7		116	95	76	76	76
8		133	114	86	86	86
9			124	95	95	95
10			133	105	105	105
11				114	114	114
12				124	124	124
13 and above				133	133	133

Note:
1. Values are guaranteed by characterization and not 100% tested in production

Table 6.8 Sequence of Bytes During Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2- … - 15-0-1-..	0-1-2- … - 31-0-1-..	0-1-2- … - 63-0-1-..
1	1-2-3- … - 15-0-1-2-..	1-2-3- … - 31-0-1-2-..	1-2-3- … - 63-0-1-2-..
….	….	….	….
15	15-0-1- … - 15-0-1-2-..	15-0-1- … - 31-0-1-2-..	15-0-1- … - 63-0-1-2-..
….	….	….	….
31	-	31-0-1- … - 31-0-1-2-..	31-0-1- … - 63-0-1-2-..
….	….	….	….
63	-	-	63-0-1- … - 63-0-1-2-..

Table 6.9 SSO (Simultaneous Switching Ouput) Pattern Selection Bit Table

SSOSEL (bit 6, 0Bh)	**IO Pattern**	**DQ0~DQ2, DQ4~DQ7**	**DQ3**
Bit 6 = 1 (default; SSO disabled)	All 8 DQs are same	0011 0101	0011 0101
Bit 6 = 0 (SSO enabled)	DQ3 is inverted (7 DQs are same)	0011 0101	1100 1010

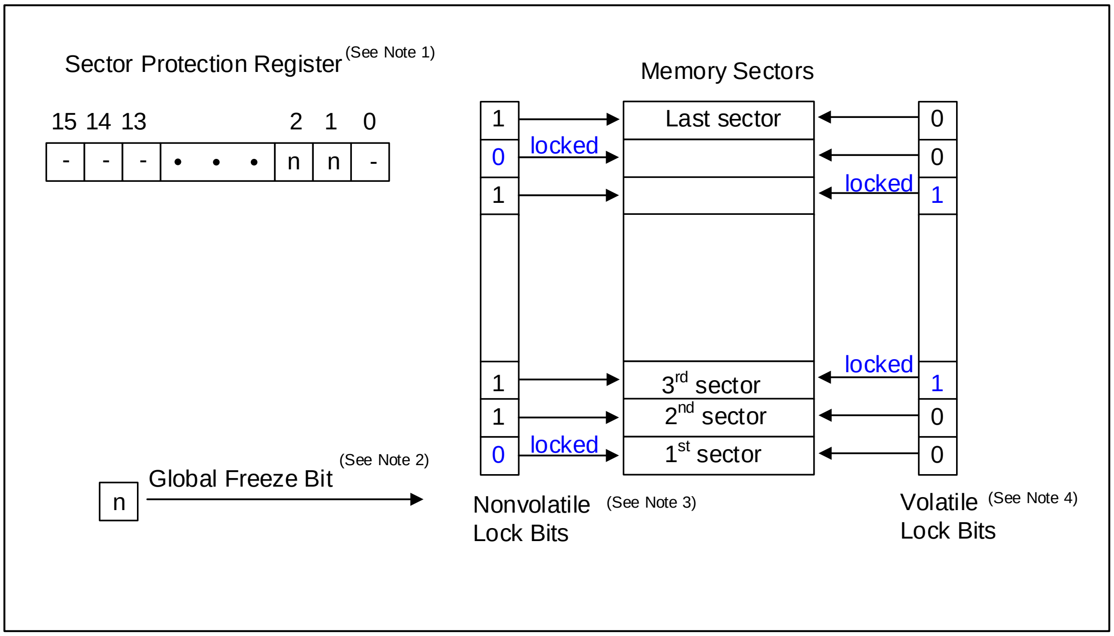
Note:
1. Training pattern can be written to DLPPTN bits (bit [7:0], address 0Ah). Bit 7 maps to 1st Training Data of MSB.

The default pattern is “0101 0101” for all 8 DQs (no SSO pattern).

6.6 SECURITY REGISTERS

Security Registers enable sector and password protection on multiple levels using non-volatile and volatile register and bit settings.

Figure 6.2 Sector and Password Protection



Notes:

1. **Sector protection register: This 16-bit nonvolatile register includes two active bits [2:1] to enable sector and password protection.**
2. **Global freeze bit:** This volatile bit protects the settings in all nonvolatile lock bits.
3. **Nonvolatile lock bits:** Each nonvolatile bit corresponds to and provides nonvolatile protection for an individual memory sector (128KB), which remains locked (protection enabled) until its corresponding bit is cleared to 1.
4. **Volatile lock bits:** Each volatile bit corresponds to and provides volatile protection for an individual memory sector (128KB), which is locked temporarily(protection is cleared when the device is reset or powered down)
5. **In an optional device of 64KB sector size, nonvolatile lock bits and volatile lock bits for ASP (Advanced Sector Protection) correspond to 128KB sector size instead of 64KB. But traditional BP protection correspond to 64KB sector size.**

Sector Protection Security Register

Table 6.10 Sector Protection Security Register

Bits	Name	Settings	Description	Notes
15:3	Reserved	1 = Default	-	
2	Password protection lock	1 = Disabled (Default) 0 = Enabled	**OTP bit:** When set to 1, and password protection is disabled. When set to 0, password protection is enabled permanently; the 64-bit password cannot be retrieved or reset.	1, 2
1	Sector protection lock	1 = Enabled, with password protection (Default) 0 = Enabled, without password protection	**OTP bit:** When set to 1, nonvolatile lock bits can be set to lock/unlock their corresponding memory sectors; bit 2 can be set to 0, enabling password protection permanently. When set to 0, nonvolatile lock bits can be set to lock/unlock their corresponding memory sectors; bit 2 must remain set to 1, disabling password protection permanently.	1, 3, 4
0	Reserved	1 = Default	-	

Notes:

1. **Bit 2 and bit 1 are user-configurable, one-time-programmable, and mutually exclusive in that only one of them can be set to 0.** It is recommended that one of the bits be set to 0 when first programming device when using Advanced Sector Protection.
2. The 64-bit password must be programmed and verified before this bit set to 0 because after it is set, password changes are not allowed, thus providing protection from malicious software. When this bit is set to 0, a 64-bit password is required to reset the global freeze bit from 0 to 1. In addition, if password is incorrect or lost, the global freeze bit can no longer be set and nonvolatile lock bits cannot be changed.
3. Whether this bit is set to 1 or 0, it enables programming or erasing nonvolatile lock bits (which provide memory sector protection). The password protection bit must be set beforehand because setting this bit will either enable password protection permanently (bit 2 = 0) or disable password protection permanently (bit 1 = 0)
4. **By default, all sectors are unlocked with device shipped from the factory**. Sectors are locked, unlocked, read, or lock down as explained in the Nonvolatile and Volatile Lock Bits table and the volatile Lock Bit Register Bit Definitions table.

Table 6.11 Global Freeze Bit

Bits	Name	Settings	Description
7:1	Reserved	0	Bit values are 0
0	Global freeze bit	1 = Disabled (Default) 0 = Enabled	**Volatile bit:** When set to 1, all nonvolatile lock bits can be set to enable or disable locking their corresponding memory sectors. When set to 0, nonvolatile lock bits are protected from PROGRAM or ERASE commands. This bit should not be set to 0 until the nonvolatile lock bits are set.

Note:

1. The READ GLOBAL FREEZE BIT command enables reading this bit. **When password protection is enabled, this bit is locked upon device power-up or reset.** It cannot be changed without the password. **After the password is entered, the UNLOCK PASSWORD command resets this bit to 1**, enabling programming or erasing the nonvolatile lock bits. After the bits are changed, the **WRITE GLOBAL FREEZE BIT command sets this bit to 0**, protecting the nonvolatile lock bits from PROGRAM or ERASE operations.

6.7 NONVOLATILE LOCK BIT AND VOLATILE LOCK BIT SECURITY REGISTERS

Table 6.12 Nonvolatile and volatile lock bits

Bit Details	Nonvolatile Lock Bit	Volatile Lock Bit
Description	Each sector of memory has one corresponding nonvolatile lock bit	Each sector of memory has one corresponding nonvolatile lock bit; this bit is the sector write lock bit described in the Volatile Lock Bit Register table.
Function	When set to 0, locks and protects its corresponding memory sector from PROGRAM or ERASE operations. Because this bit is nonvolatile, the sector remains locked, protection enabled, until the bit is cleared to 1.	When set to 1, locks and protects its corresponding memory sector from PROGRAM or ERASE operations. Because this bit is volatile, protection is temporary. The sector is unlocked, protection disabled, upon device reset or power-down.
Settings	1 = Lock disabled 0 = Lock enabled	0 = Lock disabled 1 = Lock enabled
Enabling protection	The bit is set to 0 by the WRITE NONVOLATILE LOCK BITS command, enabling protection for designated locked sectors. Programming a sector lock bit requires the typical byte program time.	When set to 1, locks and protects its corresponding memory sector from PROGRAM or ERASE operations. Because this bit is volatile, protection is temporary. The sector is unlocked, protection disabled, upon device reset or power-down.
Disabling protection	All bits are cleared to 1 by ERASE NONVOLATILE LOCK BITS command, unlocking and disabling protection, unlocking and disabling protection for all sectors simultaneously. Erasing all sector lock bits requires typical sector erase time.	All bits are cleared to 0 upon reset or power-down, unlocking and disabling protection for all sectors.
Reading the bit	Bits are read by the READ NONVOLATILE LOCK BITS command.	Bits are read by the READ VOLATILE LOCK BITS command.

NONVOLATILE LOCK BIT SECURITY REGISTER

For nonvolatile sector locking, the nonvolatile lock bits are stored in the flash cells within an erasable sector lock-bit array, hence, making this a nonvolatile locking scheme. An erased flash cell corresponds to an unlocked sector and programmed flash cell corresponds to a locked sector.

One of nonvolatile lock bit is related to each sector, **the nonvolatile lock bits are programmed individually but must be erased as a group**.

Programming nonvolatile lock bits requires the typical byte programming time. Erasing all the nonvolatile lock bits requires typical sector erase time.

Table 6.13 Nonvolatile Lock Bit Register

Nonvolatile Lock Bit Register	Protection Status
00h	Sector protected from modify operations
FFh	Sector unprotected from modify operations (default)

VOLATILE LOCK BIT SECURITY REGISTER

One volatile lock bit register is associated with each sector of memory. It enables the sector to be locked, unlocked, or locked-down with the WRITE VOLATILE LOCK BITS command, which executes only when sector lock down (bit 1) is set to 0. Each register can be read with the READ VOLATILE LOCK BITS command.

Table 6.14 Volatile lock bit register

Bits	Name	Settings	Description
7:2	Reserved	0	Bit values are 0-
1	Sector lock down	0 = lock-down disabled (Default) 1 = lock-down enabled	**Volatile bit:** Device always powers up with this bit set to 0 so that sector lock down and sector write protect bits can be set to 1. When this bit is set to 1, neither of the two volatile bits can be written to until the next power cycle, hardware, or software reset.
0	Sector write protect	0 = Write protect disabled (Default) 1 = Write protect enabled	**Volatile bit:** Device always powers up with this bit set to 0 so that PROGRAM or ERASE operations in this sector can be executed and sector content modified. When this bit is set to 1, PROGRAM and ERASE operations in this sector are not executed.

6.8 PROTECTION MANAGEMENT REGISTER

The device offers enhanced security features that can be enabled by properly setting the protection management register (PMR).

The PMR bits can be read from or written to using the READ PROTECTION MANAGEMENT REGISTER and WRITE PROTECTION MANAGEMENT REGISTER commands.

When the PMR lockdown bit (bit 2) is set to 0, the device will no longer respond to WRITE PROTECTION MANAGEMENT REGISTER commands. If this command is issued, the register will remain unchanged and the device will set an error code in flag status register bits 1 and 4.

Note: If the enhanced security features (activated through the PMR) are not going to be used, **programming bit 2 of the PMR to 0 is strongly recommended**. This prevents any future unintentional operation on this register that could result in permanent and irreversible locking of the memory sectors.

Table 6.15 Protection Management Register

Bit	Name	Settings	Description	Notes
7	Reserved	Reserved	Reserved	
6	Reserved	Reserved	Reserved	
5	Reserved	Reserved	Reserved	
4	Status Register Lock	0 = Lock 1 = Unlock (Default)	**OTP control bit:** Permanently locks the status register, further writes to SR not allowed regardless of the state of W# pin and write enable/disable bit of the status register.	
3	Reserved	Reserved	Reserved	
2	**PMR Lockdown**	**0 = Lock** **1 = Unlock (Default)**	**OTP control bit:** Permanently locks the protection management register.	
1	Nonvolatile sector lock bit register lockdown	0 = Lock 1 = Unlock (Default)	**OTP control bit:** Permanently locks the contents of the nonvolatile sector lock bit register.	1
0	Nonvolatile sector lock bit erase lock	0 = Lock 1 = Unlock (Default)	**OTP control bit:** When this bit is set to 1, the nonvolatile sector lock bit register array is erasable; otherwise, it is unerasable.	

Note:

1. **When this bit is set to 0, the nonvolatile lock bits are locked from PROGRAM and ERASE operations permanently.**

PROTECTION MANAGEMENT REGISTER Operations

Protection management register bits can be read with the READ PROTECTION MANAGEMENT REGISTER (2Bh) command. They can be programmed independently or collectively with the WRITE PROTECTION MANAGEMENT REGISTER command (68h).
The bits are one-time programmable and cannot be erased.

To initiate a READ PROTECTION MANAGEMENT command, S# is driven LOW. For extended SPI protocol, input is on DQ0, output on DQ1. For Octal DDR Protocol, input/output is on DQ [7:0]. The operation is terminated by driving S# HIGH at any time during data output.

Before a WRITE PROTECTION MANAGEMENT REGISTER command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. To initiate a command, S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. For the extended SPI and Octal DDR protocols, input is on DQ0, and DQ [7:0], respectively, followed by the data bytes. If S# is not driven HIGH, the command is not executed, error bits are not set, and the write enable latch remains set to 1. The operation is self-timed and its duration is tPPMR.

Table 6.16 Protection Management Register Operations

Operation Name	Description
READ PROTECTION MANAGEMENT REGISTER (2Bh)	The command does not require dummy cycles in extended SPI protocol, while 8 dummy cycles are necessary in Octal DDR protocol. When the register is read continuously, the same byte is output repeatedly.
WRITE PROTECTION MANAGEMENT REGISTER (68h)	When an operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0, whether the operation is successful or not. For stacked devices, it is possible to obtain the operation status by reading the flag status register a number of times corresponding to the die stacked, with S# toggled in between the READ FLAG STATUS REGISTER commands. When the operation completes, the program or erase controller bit of the flag status register is cleared to 1. The end of operation can be detected when the program or erase controller bit of the flag status register outputs 1 for all the die of the stack. When a 0 is written to any reserved field, the operation is initiated; however, uCode aborts the operation without programming any bits. Then the write enable latch bit is cleared, and the programming error bit and protection error bits are set to 1. When protection management bit 2 is set to 0 (locked), the command is not executed, the write enable latch remains set to 1, and flag status register and protection error bits are set to 1.

7. DEVICE ID DATA

The device ID data shown in the tables here is read by the READ ID and MULTIPLE I/O READ ID operations.

Table 7.1 Device ID Data

Byte#	Name	Value	Assigned by
Manufacturer ID (1 Byte total)			
1	Manufacturer ID (1 Byte)	9Dh	JEDEC
Device ID (2 Bytes total)			
2	Memory Type (1 Byte)	5Ah = 3V 5Bh = 1.8V	Manufacturer
3	Memory Density (1 Byte)	17h = 64Mb 16h = 32Mb	
Unique ID (17 Bytes total)			
4	Indicates the number of remaining ID bytes (1 Byte)	10h	Factory
5	Extended device ID (1 Byte)	See below Table 7.2	
6	Device configuration information (1 Byte)	See below Table 7.3	
7:20	Customized factory data (14 Bytes)	Unique ID code (UID)	

Table 7.2 Extended Device ID Data, First Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Device Generation 0 = 1st generation	Reserved	Reserved	Reserved	Reserved	Sector Size: **01 = Uniform 128KB** 10 = Uniform 64KB [(1)]	

Note:

1. 64KB is for optional device. See the Ordering Information for optional 64KB sector size.

Table 7.3 Device Configuration Information Data

Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Boot up protocol: 0 = Boot in SDR x1 1 = Boot in DDR x8	Reserved	

8. DEVICE OPERATION

8.1 BASIC DEVICE OPERATION

- Before a command is issued, status register should be checked to ensure device is ready for proper operation.

- When incorrect command is inserted, the device becomes standby mode and keeps the standby mode until next S# falling edge.

- When correct command is inserted, the device becomes active mode, and keeps active mode until next S# rising edge.

- While a Status Register Write operation or any Nonvolatile Register Write operation, access to any memory array is not allowed

- While a Status Register Write operation or any Nonvolatile Register Write operation, access to any memory array is not allowed

- In an optional device (option L), while Program or Erase of memory array is in progress in one bank, Fast Read Array data Command can be issued on any of the three non-busy banks (Read while Program/Erase Operation).

8.2 COMMAND SET SUMMARY

Table 8.1 Commend Set

Command	Code	Extended SPI		Octal DDR		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
Software RESET Operations							
RESET ENABLE	66h	1-0-0	0	8-0-0	0	0	0
RESET MEMORY	99h	1-0-0	0	8-0-0	0	0	0
READ ID Operations							
READ ID	9E/9Fh	1-0-1	0	8-0-8	8	0	1 to 20
READ SFDP	5Ah	1-1-1	8	8-8-8	8	3 (1)	1 ~
READ MEMORY Operations							
READ	03h	1-1-1	0	-	-	3/4 (2)	1 ~
FAST READ	0Bh	1-1-1	8	8-8-8	16	3/4 (2)	1 ~
OCTAL OUTPUT FAST READ	8Bh	1-1-8	8	8-8-8	16	3/4 (2)	1 ~
OCTAL I/O FAST READ	CBh	1-8-8	16	8-8-8	16	3/4 (2)	1 ~
DDR OCTAL OUTPUT FAST READ	9Dh	1-1-8	8	8-8-8	16	3/4 (2)	1 ~
DDR OCTAL I/O FAST READ	FDh	1-8-8	16	8-8-8	16	4	1 ~
READ MEMORY Operations with 4-Byte Address							
4-BYTE READ	13h	1-1-1	0	-	-	4	1 ~
4-BYTE FAST READ	0Ch	1-1-1	8	8-8-8	16	4	1 ~
4-BYTE OCTAL OUTPUT FAST READ	7Ch	1-1-8	8	8-8-8	16	4	1 ~
4-BYTE OCTAL I/O FAST READ	CCh	1-8-8	16	8-8-8	16	4	1 ~
WRITE Operations							
WRITE ENABLE	06h	1-0-0	0	8-0-0	0	0	0
WRITE DISABLE	04h	1-0-0	0	8-0-0	0	0	0
READ REGISTER Operations							
READ STATUS REGISTER	05h	1-0-1	0	8-0-8	8	0	1 ~
READ FLAG STATUS REGISTER	70h	1-0-1	0	8-0-8	8	0	1 ~
READ NONVOLATILE CONFIGURATION REGISTER	B5h	1-1-1	8	8-8-8	8	3/4 (2)	1 ~
READ VOLATILE CONFIGURATION REGISTER	85h	1-1-1	8	8-8-8	8	3/4 (2)	1 ~
READ PROTECTION MANAGEMENT REGISTER	2Bh	1-0-1	0	8-0-8	8	0	1 ~

Command Set (Continued)

Command	Code	Extended SPI		Octal DDR		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
WRITE REGISTER Operations							
WRITE STATUS REGISTER	01h	1-0-1	0	8-0-8	0	0	1
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	1-1-1	0	8-8-8	0	3/4 (2)	1
WRITE VOLATILE CONFIGURATION REGISTER	81h	1-1-1	0	8-8-8	0	3/4 (2)	1
WRITE PROTECTION MANAGEMENT REGISTER	68h	1-0-1	8	8-0-8	0	0	1
CLEAR Operations							
CLEAR FLAG STATUS REGISTER	50h	1-0-0	0	8-0-0	0	0	0
CLEAR ERRB	B6h	1-0-0	0	8-0-0	0	0	0
PROGRAM Operations							
PAGE PROGRAM	02h	1-1-1	0	8-8-8	0	3/4 (2)	1 to 256
OCTAL INPUT FAST PROGRAM	82h	1-1-8	0	8-8-8	0	3/4 (2)	1 to 256
EXTENDED OCTAL INPUT FAST PROGRAM	C2h	1-8-8	0	8-8-8	0	3/4 (2)	1 to 256
PROGRAM Operations with 4-BYTE Address							
4-BYTE PAGE PROGRAM	12h	1-1-1	0	8-8-8	0	4	1 to 256
4-BYTE OCTAL INPUT FAST PROGRAM	84h	1-1-8	0	8-8-8	0	4	1 to 256
4-BYTE EXTENDED OCTAL INPUT FAST PROGRAM	8Eh	1-8-8	0	8-8-8	0	4	1 to 256
ERASE Operations							
32KB SUBSECTOR ERASE	52h	1-1-0	0	8-8-0	0	3/4 (2)	0
4KB SUBSECTOR ERASE	20h	1-1-0	0	8-8-0	0	3/4 (2)	0
128KB SECTOR ERASE	D8h	1-1-0	0	8-8-0	0	3/4 (2)	0
CHIP ERASE	C7h/60h	1-0-0	0	8-0-0	0	0	0
ERASE Operations with 4-BYTE Address							
4-BYTE 32KB SUBSECTOR ERASE	5Ch	1-1-0	0	8-8-0	0	4	0
4-BYTE 4KB SUBSECTOR ERASE	21h	1-1-0	0	8-8-0	0	4	0
4-BYTE 128KB SECTOR ERASE	DCh	1-1-0	0	8-8-0	0	4	0
SUSPEND/RESUME Operations							
PROGRAM/ERASE SUSPEND	75h	1-0-0	0	8-0-0	0	0	0
PROGRAM/ERASE RESUME	7Ah	1-0-0	0	8-0-0	0	0	0
ONE-TIME PROGRAMMABLE (OTP) Operations							
READ OTP ARRAY	4Bh	1-1-1	8	8-8-8	16	3/4 (2)	1 to 65
PROGRAM OTP ARRAY	42h	1-1-1	0	8-8-8	0	3/4 (2)	1 to 65

Commend Set (Continued)

Command	Code	Extended SPI		Octal DDR		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
4-BYTE ADDRESS MODE Operations							
ENTER 4-BYTE ADDRESS MODE	B7h	1-0-0	0	-(5)	-5)	0	1
EXIT 4-BYTE ADDRESS MODE	E9h	1-0-0	0	- (5)	-(5)	0	1
DEEP POWER-DOWN Operations							
ENTER DEEP POWER-DOWN	B9h	1-0-0	0	8-0-0	0	0	0
RELEASE FROM DEEP POWER-DOWN	ABh	1-0-0	0	8-0-0	0	0	0
ADVANCED SECTOR PROTECTION Operations							
READ SECTOR PROTECTION	2Dh	1-0-1	0	8-0-8	8	0	1 ~
PROGRAM SECTOR PROTECTION	2Ch	1-0-1	0	8-0-8	0	0	2
READ VOLATILE LOCK BITS	E8h	1-1-1	0	8-8-8	8	3/4 (2)	1 ~
WRITE VOLATILE LOCK BITS	E5h	1-1-1	0	8-8-8	0	3/4 (2)	1
READ NONVOLATILE LOCK BITS	E2h	1-1-1	0	8-8-8	8	4	1 ~
WRITE NONVOLATILE LOCK BITS	E3h	1-1-0	0	8-8-0	0	4	0
ERASE NONVOLATILE LOCK BITS	E4h	1-0-0	0	8-0-0	0	0	0
READ GLOBAL FREEZE BIT	A7h	1-0-1	0	8-0-8	8	0	1 ~
WRITE GLOBAL FREEZE BIT	A6h	1-0-0	0	8-0-0	0	0	0
READ PASSWORD	27h(3)	1-0-1	0	8-0-8	8	0	1 ~
WRITE PASSWORD	28h	1-0-1	0	8-0-8	0	0	8
UNLOCK PASSWORD	29h	1-0-1	0	8-0-8	0	0	8
ADVANCED SECTOR PROTECTION Operations with 4-BYTE Address							
4-BYTE READ VOLATILE LOCK BITS	E0h	1-1-1	0	8-8-8	8	4	1 ~
4-BYTE WRITE VOLATILE LOCK BITS	E1h	1-1-1	0	8-8-8	0	4	1
DATA LEARNING PATTERN Operations							
DATA LEARNING PATTERN READ	CDh	1-0-8	18(4)	8-0-8	18(4)	0	1~

Notes:

1. **Read SFDP instruction accepts only 3-byte address even if the device is configured to 4-byte address mode. In Octal DDR mode, it will be fixed 4-byte address cycle.**
2. **Requires 4-byte of address if the device is configured to 4-byte address mode or Octal DDR protocol.**
3. **After the 8-bit instruction shifted in, the 64-bit data are shifted out, the last significant byte first, most significant bit of each byte first. The READ PASSWORD instruction is terminated by driving chip select (S#) HIGH at any time during data output. When read continuously, the device outputs 64-bit data repeatedly.**
4. **Dummy cycle for DLP READ operation is set by 01h of configuration register setting.
   Dummy cycle for DLP READ = Dummy cycle setting of OCTAL DDR mode + 2 clock cycles. 18 clock cycle is a default setting.**
5. **If the device is configured to Octal DDR mode, it will be fixed 4-byte address mode regardless of B7h, E9h command.**

8.3 SOFTWARE RESET OPERATIONS

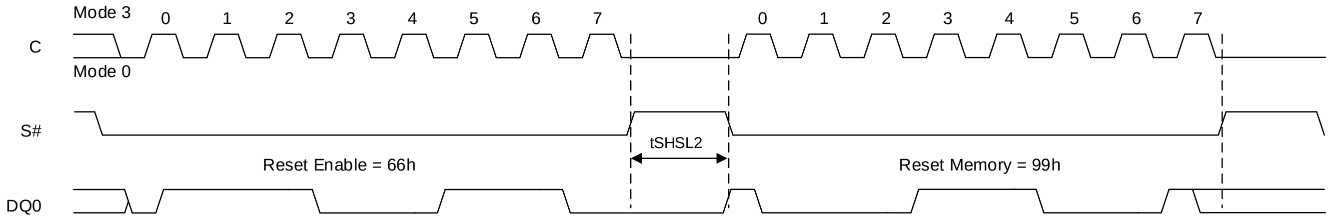
RESET ENABLE and RESET MEMORY Commands

To initiate these commands, S# is driven LOW and the command code is input on DQ0. A minimum de-selection time of tSHSL2 must come between RESET ENABLE and RESET MEMORY or reset is not guaranteed. Then, S# must be driven HIGH for the device to enter power-on reset.

Table 8.2 RESET ENABLE and RESET MEMORY Commands

Operation Name	Description/Conditions
RESET ENABLE (66h)	To reset the device, the RESET ENABLE command must be followed by the RESET MEMORY command. When the two commands are executed, the device enters a power-on reset condition. It is recommended to XIP mode before executing these two commands. All volatile lock bits and volatile configuration register are reset to the power-on reset default condition according to nonvolatile configuration register settings. If a reset is initiated while a WRITE, PROGRAM, or ERASE operation is in progress or suspended, the operation is aborted and data may be corrupted. **Reset is effective after the flag status register bit 7 outputs 1 with at least one byte output**.
RESET MEMORY (99h)	

Figure 8.1 RESET ENABLE and RESET MEMORY – 66h and 99h



Note:

1. **The Octal DDR protocol uses eight data pins to transmit information.**

8.4 READ ID OPERATION

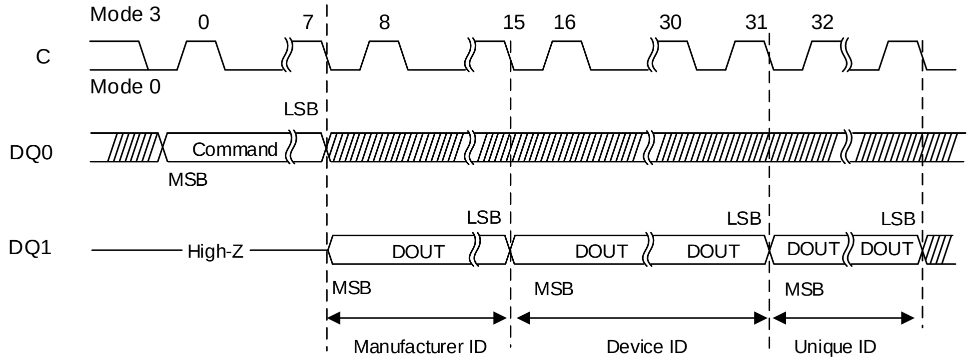
To initiate this command, S# is driven LOW and the command code is input on DQn. When S# is driven HIGH, the device goes to standby. The operation is terminated by driving S# HIGH at any time during data output.

Table 8.3 READ ID Operation

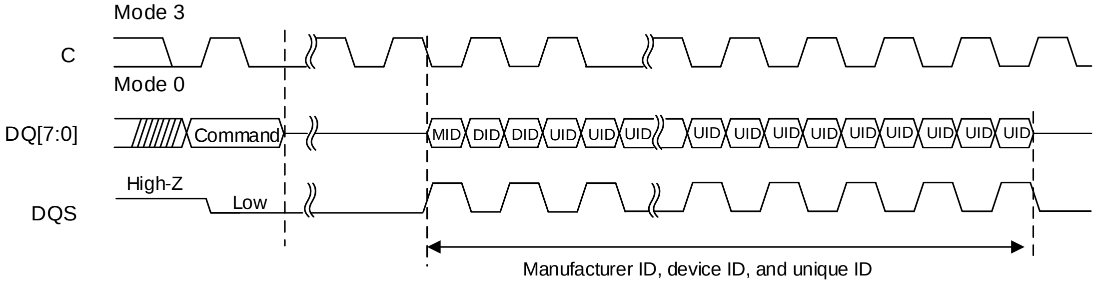
Operation Name	Description/Conditions
READ ID (9Eh/9Fh)	Outputs information shown in the Device ID Data tables. If an ERASE or PROGRAM cycle is in progress when the command is initiated, the command is not decoded and the command cycle in progress is not affected.

Figure 8.2 READ ID Command

Extended



Octal DDR



Note:

1. **S# not shown.**

8.5 READ SFDP OPERATION

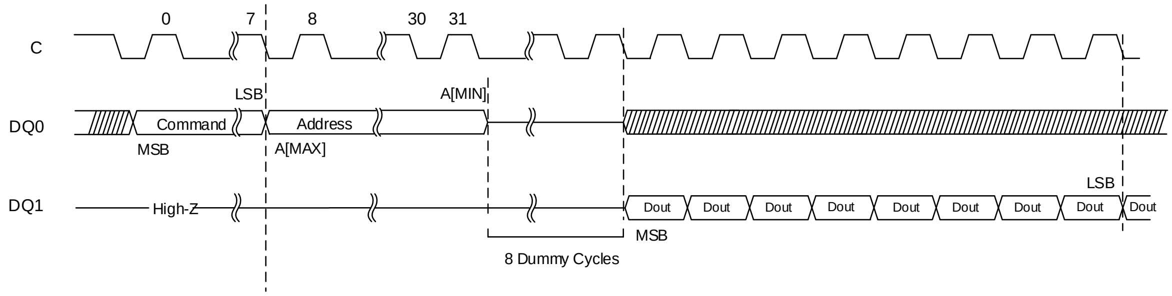
Read SFDP (Serial Flash Discovery Parameter) Command

To execute READ SFDP command, S# is driven LOW. The command code is input on DQ0, followed by three address bytes and eight dummy clock cycles. The device outputs the information starting from the specified address. When 256-byte boundary reached, the data output wraps to address 0 of SFDP table. The operation is terminated by driving S# HIGH at any time during data output.

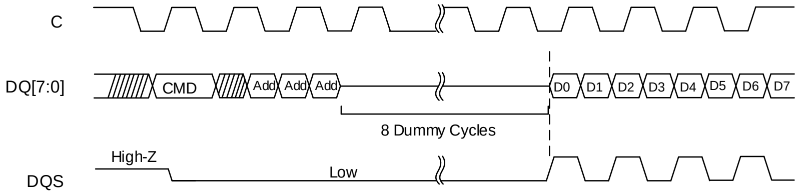
Note: The operation always executes in continuous mode so the read burst wrap setting in the volatile configuration register does not apply.

Figure 8.3 READ SFDP Command – 5Ah

Extended



Octal DDR



Note:
1. **S# not shown.**

8.6 READ MEMORY OPERATION

To initiate a command, S# is driven LOW and the command code is input on DQn, followed by input of the address bytes on DQn. The operation is terminated by driving S# HIGH at any time during data output.

Table 8.4 READ MEMORY Operation

Operation Name		**Description/Conditions**
READ (03h)	1S-1S-1S	The device supports 3-byte addressing (default), with A [23:0] input during address cycle. After any READ command is executed, the device will output data from the selected address. After the boundary is reached, the device will start reading again from the beginning. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of data is shifted out; therefore, a die can be read with a single command. FAST READ can operate at higher frequency (fC). DDR commands function in DDR protocol regardless of settings in the nonvolatile configuration register; Other commands function in DDR protocol only after DDR protocol is enabled by the register settings. **Due to the nature of DDR protocol, an even number of bytes is always transferred**. **The LSB of the byte address shall always be zero when using DDR protocol**. If LSB of the address is set to one when using DDR protocol, the results are indeterminate.
FAST READ (0Bh)	1S-1S-1S	
OCTAL OUTPUT FAST READ (8Bh)	1S-1S-8S	
OCTAL I/O FAST READ (CBh)	1S-8S-8S	
DDR OCTAL OUTPUT FAST READ(9Dh)	1S-1D-8D	

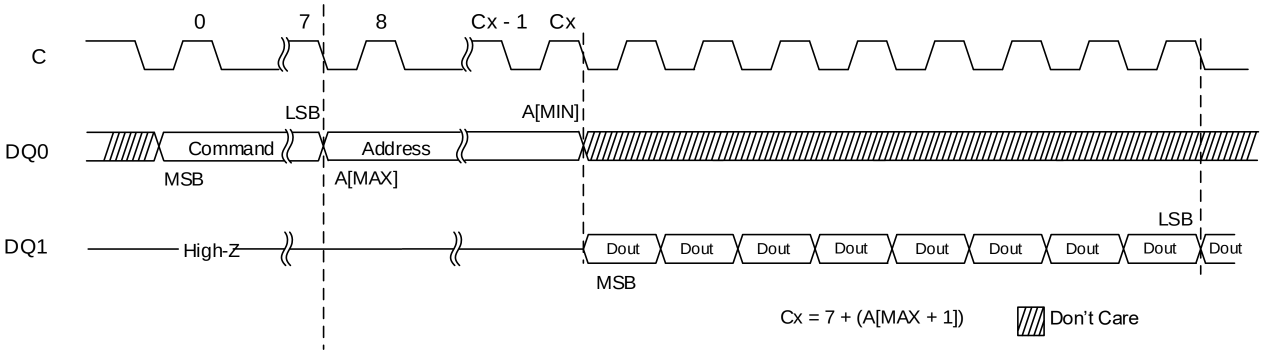
4-BYTE READ MEMORY Operations

Table 8.5 4-BYTE READ MEMORY Operation

Operation Name		**Description/Conditions**
4-BYTE READ (13h)	1S-1S-1S	READ MEMORY operations can be extended to a 4-byte address range, with A [31:0] input during address cycle. Selection of 3-byte or 4-byte address can be enabled in two ways: through nonvolatile configuration register or through the ENABLE 4-BYTE ADDRESS MODE/EXIT 4-BYTE ADDRESS MODE commands. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of the data is shifted out; therefore, a die can be read with a single command. FAST READ can operate at higher frequency (fC)
4-BYTE FAST READ (0Ch)	1S-1S-1S	
4-BYTE OCTAL OUTPUT FAST READ (7Ch)	1S-1S-8S	
4-BYTE OCTAL I/O FAST READ (CCh)	1S-8S-8S	
DDR OCTAL I/O FAST READ [1] (FDh)	1S-8D-8D	

READ MEMORY Operations Timings

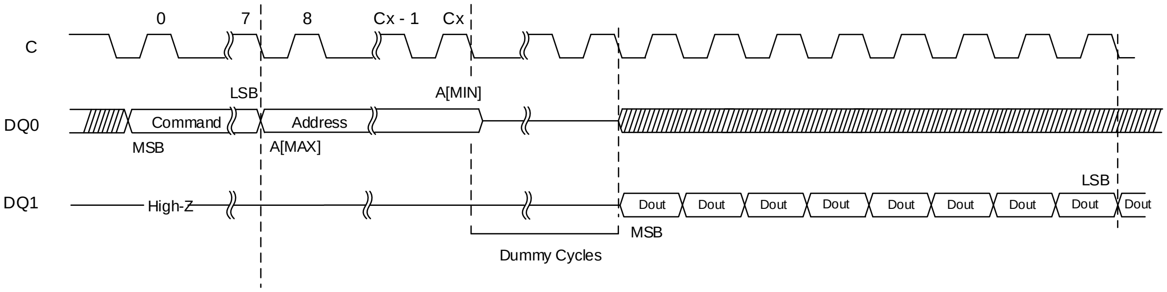
Figure 8.4 SDR READ (1S-1S-1S) – 03h/13h (2)



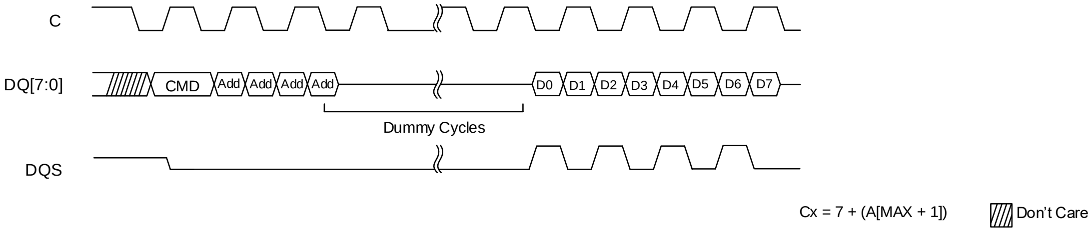
Notes:
1. S# not shown.
2. READ and 4-BYTE READ COMMANDS

Figure 8.5 FAST READ – 0Bh/0Ch (3)

Extended

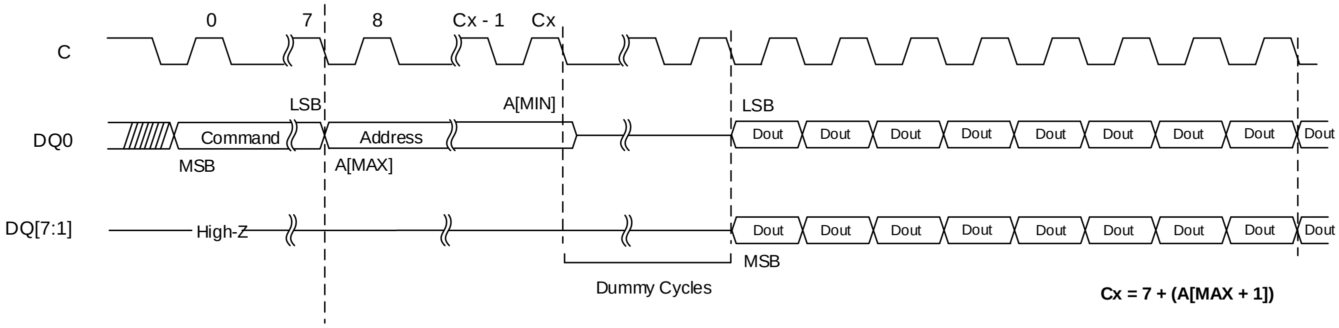


Octal DDR



Notes:
1. Timing shows command code 0Bh but this timing also applies to the following DDR protocol command codes, for which device behavior is identical: 8Bh, CBh, 9Dh, FDh, 7Ch, and CCh.
2. S# not shown
3. FAST READ and 4-BYTE FAST READ COMMANDS

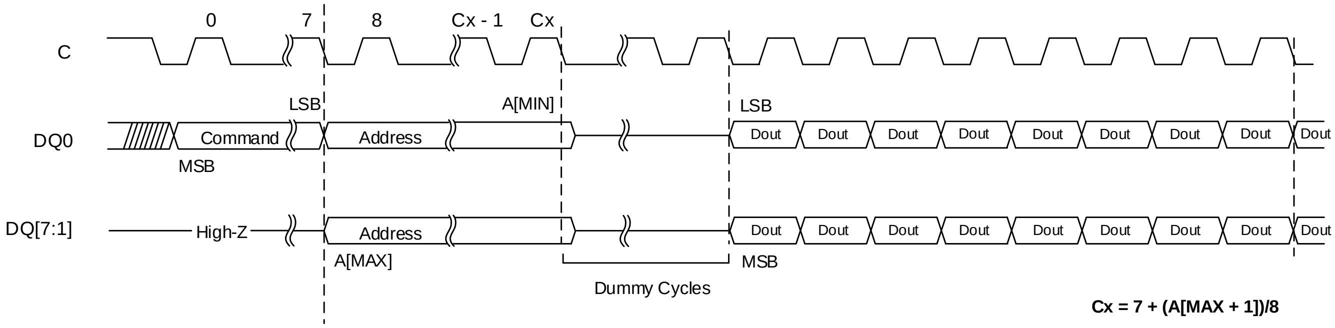
Figure 8.6 OCTAL OUTPUT FAST READ (1S-1S-8S) – 8Bh/7Ch [3]



Notes:

1. **Requires 32-bit address in 4-byte address configuration. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode.**
   The address is fixed with 4-byte.
2. **S# not shown**
3. **OCTAL OUTPUT FAST READ and 4-BYTE OCTAL OUTPUT FAST READ COMMANDS**

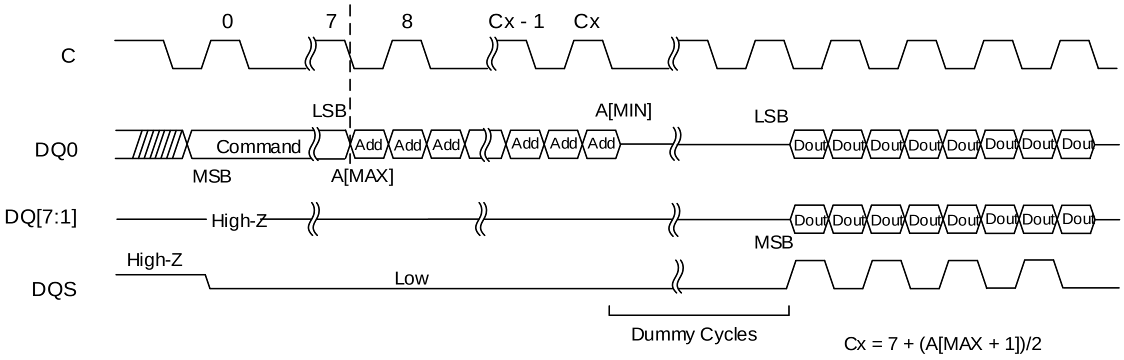
Figure 8.7 OCTAL I/O FAST READ (1S-8S-8S) – CBh/CCh [3]



Notes:

1. **Requires 32-bit address in 4-byte address configuration. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode.**
   The address is fixed with 4-byte.
2. **S# not shown**
3. **OCTAL I/O FAST READ and 4-BYTE OCTAL I/O FAST READ COMMANDS**

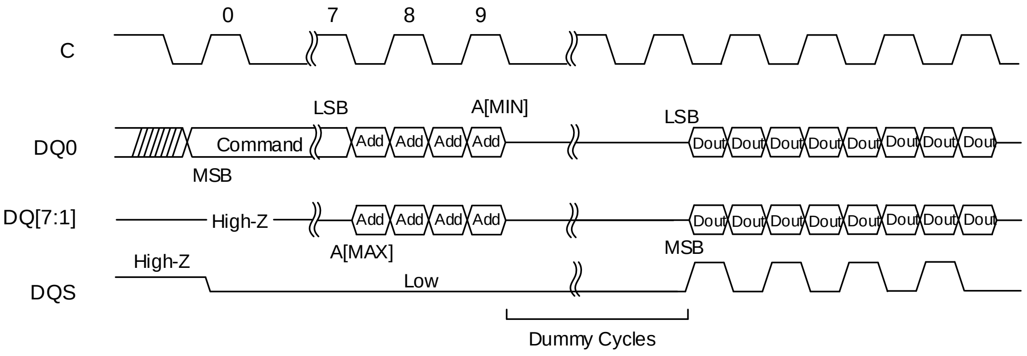
Figure 8.8 DDR OCTAL OUTPUT FAST READ with DDR ADDRESS and DATA (1S-1D-8D)– 9Dh[3]



Notes:

1. **Requires 32-bit address in 4-byte address configuration. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode.**
   The address is fixed with 4-byte.
2. **S# not shown**
3. **DDR OCTAL OUTPUT FAST READ COMMAND. No 4-BYTE DDR OCTAL I/O FAST READ COMMAND.**

Figure 8.9 4-BYTE DDR OCTAL I/O FAST READ with DDR ADDRESS and DATA (1S-8D-8D) – FDh[1]



Notes:

1. **FDh (DDR OCTAL I/O FAST READ COMMAND) is 4-Byte Address command. Always requires 32-bit address. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode.**
2. **S# not shown**

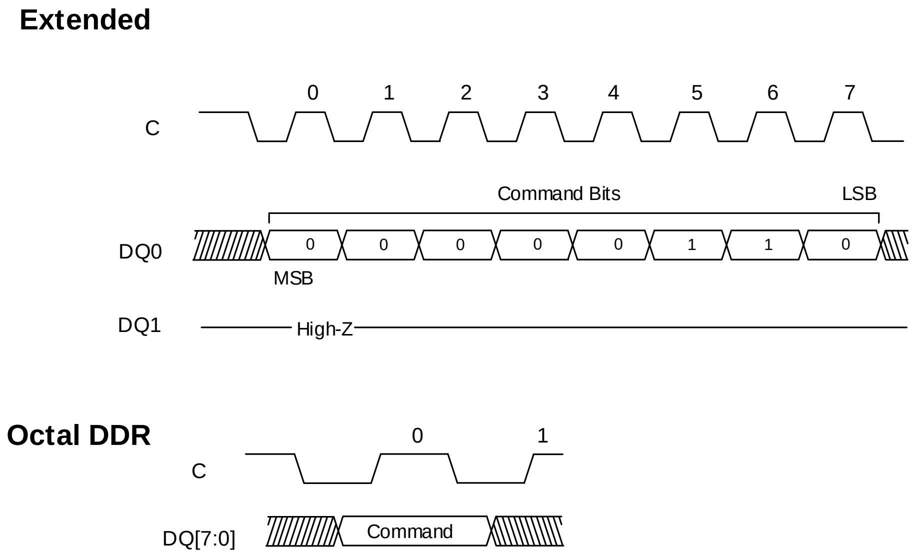
8.7 WRITE ENABLE/DISABLE OPERATION

To initiate a command, S# is driven LOW and held LOW until the eight bit of the command code has been latched in, after which it must be driven HIGH. For extended and Octal SPI protocols respectively, the command code is input on DQ0 and DQ [7:0]. If S# is not driven HIGH after the command code has been latched in, the command is not executed, flag status register error bits are not set, and the write enable latch remains cleared to its default setting of 0, providing protection against errant data modification.

Table 8.6 WRITE ENABLE/DISABLE Operation

Operation Name	Description/Conditions
WRITE ENABLE	Sets the write enable latch bit before each PROGRAM, ERASE, and WRITE command
WRITE DISABLE	Clears the write enable latch bit. In case of a protection error, WRITE DISABLE will not clear the bit. Instead, a CLEAR FLAG STATUS REGISTER command must be issued to clear both flags.

Figure 8.10 WRITE ENABLE and WRITE DISABLE Timing



Notes:

1. **WRITE ENABLE command sequence and code, shown here, is 06h (0000 0110 binary). WRITE DISABLE timing is identical, but its command code is 04h (0000 0100 binary).**

8.8 READ REGISTER OPERATION

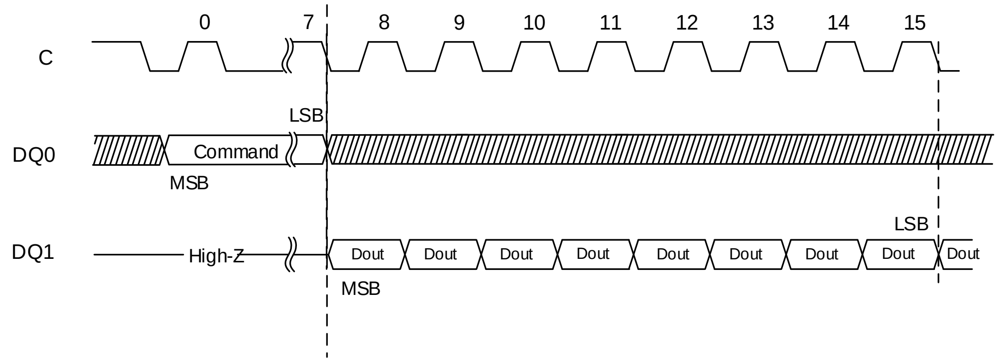
To initiate a command, S# is driven LOW. For extended SPI protocol, input is on DQ0, output on DQ1. For octal SPI protocol, I/O is on DQ [7:0]. The operation is terminated by driving S# HIGH at any time during data output.

Table 8.7 READ REGISTER Operations

Operation Name	Description/Conditions
READ STATUS REGISTER (05h)	Can be read continuously and at any time, including during a PROGRAM, ERASE, or WRITE OPERATION. If one of these operations is in progress, checking the write in progress bit or P/E controller bit is recommended before executing the command.
READ FLAG STATUS REGISTER (70h)	
READ NONVOLATILE CONFIGURATION REGISTER (B5h)	When continuously read, the device outputs the same byte repeatedly. All reserved fields output a value of 1.
READ VOLATILE CONFIGURATION REGISTER (85h)	When continuously read, the device outputs the same byte repeatedly. All reserved fields output a value of 1.

Figure 8.11 READ STATUS REGISTER – 05h

Extended



Octal DDR

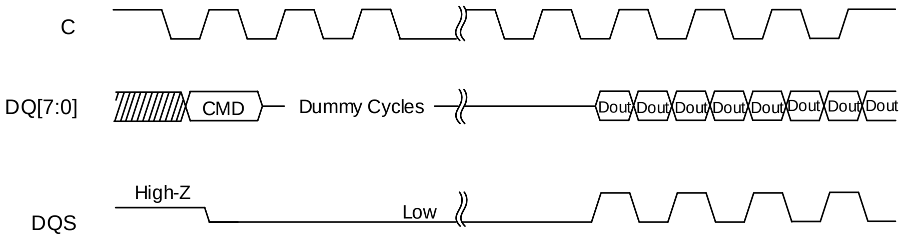
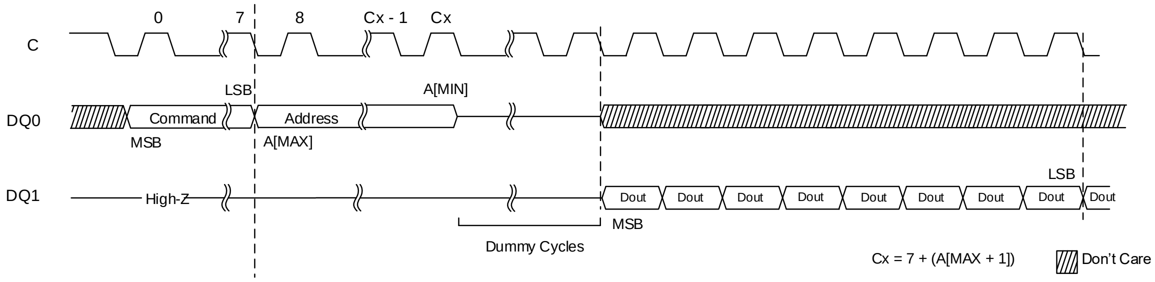
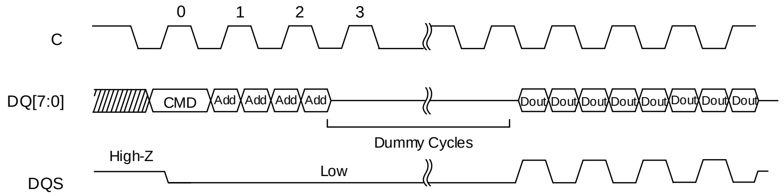


Figure 8.12 READ CONFIGURATION REGISTER – B5h/85h

Extended



Octal DDR



Notes:

1. **S# not shown.**
2. **Requires 4-bytes of address if device is configured to 4-byte address mode.**

8.9 WRITE REGISTER OPERATION

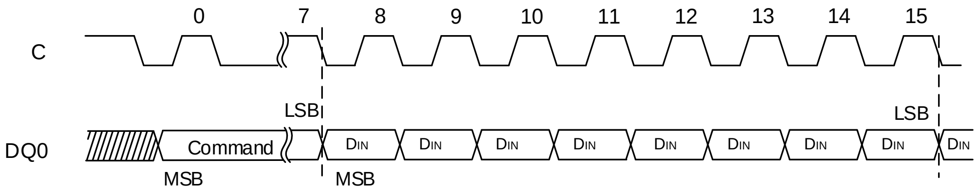
Before a WRITE REGISTER command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. To initiate a command, S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH; for the WRITE NONVOLATILE CONFIGURATION REGISTER command. For the extended and octal SPI protocols respectively, input is on DQ0 and DQ [7:0], followed by the data bytes. If S# is not driven HIGH, the command is not executed, flag status register bits are not set, and the write enable latch remains set to 1. The operation is self-timed and its duration is tW for WRITE STATUS REGISTER and tNVCR for WRITE NONVOLATILE CONFIGURATION REGISTER.

Table 8.8 WRITE REGISTER Operations

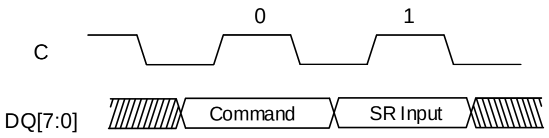
Operation Name	Description/Conditions
WRITE STATUS REGISTER (01h)	The WRITE STATUS REGISTER command writes new values to status register bits 7:2, enabling software data protection. The status register can also be combined with the W# signal to provide hardware data protection. This command has no effect on status register bits 1:0. For the WRITE STATUS REGISTER and WRITE NONVOLATILE CONFIGURATION REGISTER commands, when the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag staus register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0, whether the operation is successful or not.
WRITE NONVOLATILE CONFIGURATION REGISTER (B1h)	
WRITE VOLATILE CONFIGURATION REGISTER (81h)	Because register bits are volatile, change to this bit is immediate. Reserved bits are not affected by this command.

Figure 8.13 WRITE STATUS REGISTER – 01h

Extended



Octal DDR

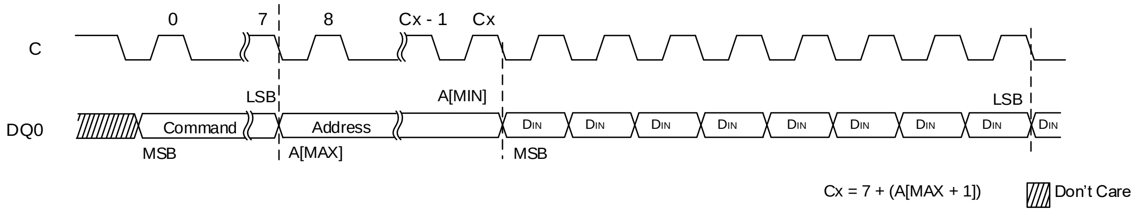


Note:

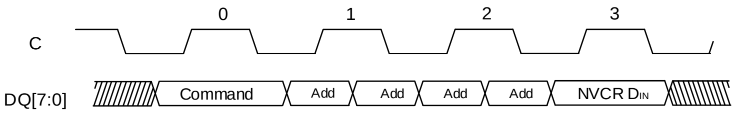
1. **S# not shown.**

Figure 8.14 WRITE CONFIGURATION REGISTER – B1h/81h

Extended



Octal DDR



Notes:

1. **S# not shown.**
2. **Requires 4-bytes of address if device is configured to 4-byte address mode.**

8.10 CLEAR FLAG STATUS REGISTER OPERATION

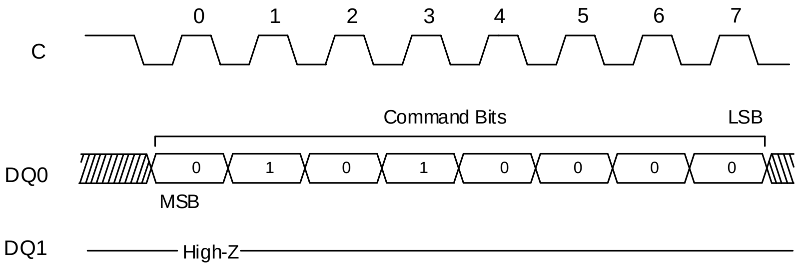
To initiate a command, S# is driven LOW. For extended SPI protocol, input is on DQ0, output on DQ1. For octal SPI protocol, I/O is on DQ [7:0]. The operation is terminated by driving S# HIGH at any time.

Table 8.9 WRITE REGISTER Operations

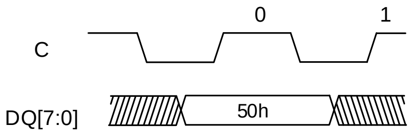
Operation Name	Description/Conditions
CLEAR FLAG STATUS REGISTER (50h)	Resets the error bits (erase, program, and protection)

Figure 8.15 CLEAR FLAG STATUS REGISTER Timing – 50h

Extended



Octal DDR



Note:

1. S# not shown.

8.11 PROGRAM OPERATION

Before a PROGRAM command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. To initiate a command, S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. Each address bit is latched in during the rising edge of the clock. When a command is applied to a protected sector, the command is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set. If the operation times out, the write enable latch bit is reset and the program fail bit is set to 1.

Note: The manner of latching data shown and explained in the timing diagrams ensures that the number of clock pulses is a multiple of one byte before command execution, helping reduce the effects of noisy or undesirable signals and enhancing device data protection.

Table 8.10 PROGRAM Operations

Operation Name	Description/Conditions
PAGE PROGRAM (02h)	A PROGRAM operation changes a bit from 1 to 0. When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0. An operation can be paused or resumed by the PROGRAM/ERASE SUSPEND or PROGRAM/ERASE RESUME command, respectively. If the bits of the least significant address, which is the starting address, are not all zero, all data transmitted beyond the end of the current page is programmed from the starting address of the same page. If the number of bytes sent to the device exceed the maximum page size, previously latched data is discarded and only the last maximum page-size number of data bytes are guaranteed to be programmed correctly within the same page. If the number of bytes sent to the device is less than the maximum page size, they are correctly programmed at the specified address without any effect on the other bytes of the same page. Due to its nature, Octal DDR operation requires bus transition in **even number**, therefore for program operation, the following restriction apply: - If there is a need to program from odd starting address, keep the even input address and the input data shall start with “FFh”. - - If there is a need to program with odd ending address, simply provide an extra data with “FFh” in the last falling edge of clock.
OCTAL INPUT FAST PROGRAM (82h)	
EXTENDED OCTAL INPUT FAST PROGRAM (C2h)	

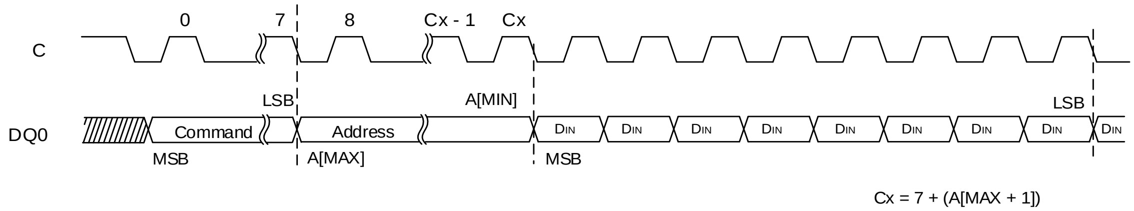
4-BYTE PROGRAM Operations

Table 8.11 4-BYTE PROGRAM Operations

Operation Name	Description/Conditions
4-BYTE PAGE PROGRAM (12h)	PROGRAM operations can be extended to a 4-bytes address range, with [A31:0] input during address cycle. Selecton of the 3-byte or 4-byte address range can be enabled in two ways: - through the nonvolatile configuration register. - through the ENABLE 4-BYTE ADDRESS MODE/EXIT 4-BYTE ADDRESS MODE commands.
4-BYTE OCTAL INPUT FAST PROGRAM (84h)	
4-BYTE EXTENDED OCTAL INPUT FAST PROGRAM (8Eh)	

Figure 8.16 PAGE PROGRAM – 02h/12h

Extended

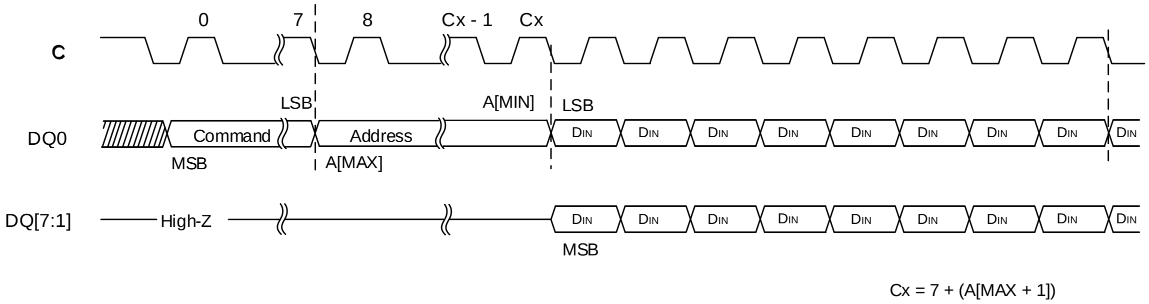


Notes:

1. **Request 4-bytes of address if device is configured to 4-byte address mode.**
2. **In Octal DDR protocol, command, address, and data-input bits are transmitted on all eight DQ pins in DDR mode, and address is fixed with 4-byte mode.**
3. **S# is not shown. The operation is self-timed, and its duration is tPP.**

Figure 8.17 OCTAL INPUT FAST PROGRAM – 82h/84h

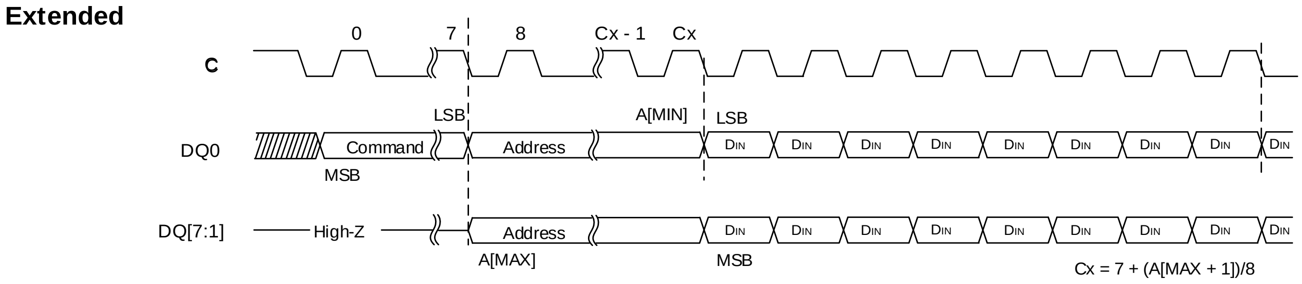
Extended



Notes:

1. **Requires 4-bytes of address if device is configured to 4-byte address mode.**
2. **In Octal DDR protocol, command, address, and data-input bits are transmitted on all eight DQ pins in DDR mode, and address is fixed with 4-byte mode.**
3. **S# is not shown. The operation is self-timed, and its duration is tPP.**

Figure 8.18 EXTENDED OCTAL INPUT FAST PROGRAM – C2h/8Eh



Notes:

1. **Requires 4-bytes of address if device is configured to 4-byte address mode.**
2. **In Octal DDR protocol, command, address, and data-input bits are transmitted on all eight DQ pins in DDR mode, and address is fixed with 4-byte mode.**
3. **S# is not shown. The operation is self-timed, and its duration is tPP.**

8.12 ERASE OPERATION

An ERASE operation changes a bit from 0 to 1. Before any ERASE command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1; if not, the device ignores the command and no error bits are set to indicate operation failure. S# is driven LOW and held LOW until eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The operations are self-timed, and duration is tSSE, tSE, or tBE according to command.

If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. A command applied to a protected subsector is not executed. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. In addition, the write in progress bit is set to 1. When the operation completes, the write in progress bit is cleared to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. If the operation times out, the write enable latch bit is reset and the erase error bit is set to 1.

The status register and flag status register can be polled for the operation status. When the operation completes, these register bits are cleared to 1.

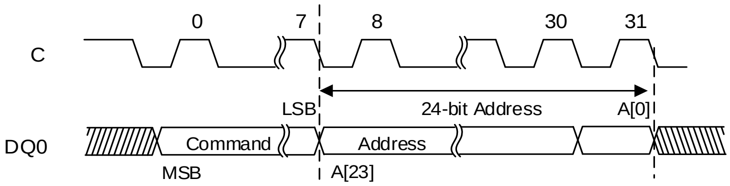
Note: For all ERASE operations, noisy or undesirable signal effects can be reduced and device data protection enhanced by holding S# LOW until the eighth bit of the last data byte has been latched in; this ensures that the number of clock pulses is a multiple of one byte before command execution

Table 8.12 ERASE Operations

Operation Name	Description/Conditions
SUBSECTOR ERASE (52h/20h)	Sets the selected subsector or sector bits to FFh. Any address within the subsector is valid for entry. Each address bit is latched in during the rising edge of the clock. The operation can be suspended and resumed by the PROGRAM/ERASE SUSPEND and PROGRAM/ERASE RESUME commands, respectively.
SUBSECTOR ERASE (D8h)	
CHIP ERASE (C7h/60h)	Sets the device bits to FFh. The command is not executed if any sector is locked. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

Figure 8.19 SUBSECTOR and SECTOR ERASE Timing

Extended

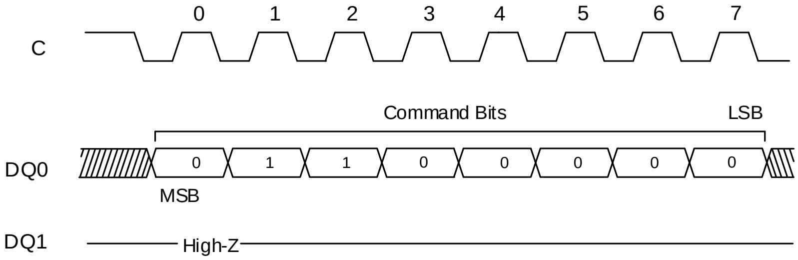


Notes:

1. **Requires 4-bytes of address if device is configured to 4-byte address mode.**
2. **In Octal DDR protocol, command, address, and data-input bits are transmitted on all eight DQ pins in DDR mode, and address is fixed with 4-byte mode.**
3. **S# is not shown. The operation is self-timed, and its duration is tSSE/tSE.**

Figure 8.20 CHIP ERASE Timing

Extended



Notes:

1. **In Octal DDR protocol, command, address, and data-input bits are transmitted on all eight DQ pins in DDR mode.**
2. **S# is not shown. The operation is self-timed, and its duration is tBE.**

8.13 SUSPEND/RESUME OPERATIONS

PROGRAM/ERASE SUSPEND Operations

A PROGRAM/ERASE SUSPEND command enables the memory controller to interrupt and suspend an array PROGRAM or ERASE operation within the program/erase latency.
To initiate the command, S# is driven LOW, and the command code is input on DQn. The operation is terminated by the PROGRAM/ERASE RESUME command.

For a PROGRAM SUSPEND, the flag status register bit 2 is set to 1. For an ERASE SUSPEND, the flag status register bit 6 is set to 1.

After an erase/program latency time, the flag status register bit 7 is also set to 1, but the device is considered in suspended state once bit 7 of the flag status register outputs 1 with at least one byte output. In the suspended state, the device is waiting for any operation.

If the time remaining to complete the operation is less than the suspend latency, the device completes the operation and clears the flag status register bits 2 or 6, as applicable. Because the suspend state is volatile, if there is a power cycle, the suspend state information is lost and the flag status register powers up as 80h.

It is possible to nest a PROGRAM/ERASE SUSPEND operation inside a PROGRAM/ERASE SUSPEND operation just once. Issue an ERASE command and suspend it. Then issue a PROGRAM command and suspend it also. With the two operations suspended, the next PROGRAM/ERASE RESUME command resumes the latter operation, and a second PROGRAM/ERASE RESUME command resumes the former (or first) operation.

Table 8.13 SUSPEND Operations

Operation Name	**Description/Conditions**
PROGRAM SUSPEND (75h)	A READ operation is possible in any page except the one in a suspended state. Reading from a sector that is in a suspended state will output indeterminate data.
ERASE SUSPEND (75h)	A PROGRAM or READ operation is possible in any page except the one in a suspended state. Reading from a sector that is in a suspended state will output indeterminate data. During a SUSPEND SUBSECTOR ERASE operation, reading an address in the sector that contains the suspended subsector could output indeterminate data. The device ignores a PROGRAM command to a sector that is in an erase suspend state; it also sets the flag status register bit 4 to 1 (program failure/protection error) and leaves the write enable latch bit unchanged. When the ERASE resumes, it does not check the new lock status of the WRITE VOLATILE LOCK BITS command.

PROGRAM/ERASE RESUME Operations

To initiate the command, S# is driven LOW, and the command code is input on DQn. The operation is terminated by driving S# HIGH.

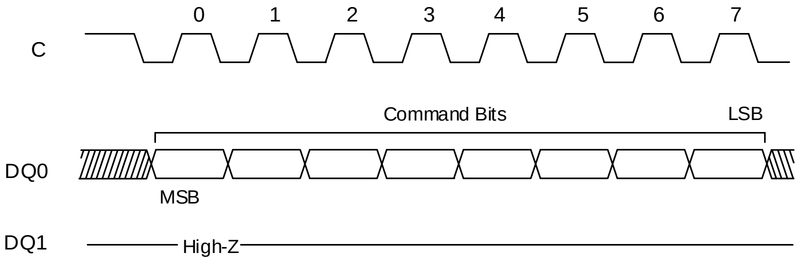
Table 8.14 RESUME Operations

Operation Name	**Description/Conditions**
PROGRAM RESUME (7Ah)	The status register write in progress bit is set to 1 and the flag status register program erase controller bit is set to 0. The command is ignored if the device is not in a suspended state. When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The flag status register can be polled for the operation status. When the operation completes, that bit is cleared to 1.
ERASE RESUME (7Ah)	

Note:
3. **See the Operations Allowed/Disallowed During Device States table.**

Figure 8.21 PROGRAM/ERASE SUSPEND or RESUME Timing

Extended



Notes:
1. **In Octal DDR protocol, command is transmitted on all eight DQ pins.**
2. **S# is not shown.**

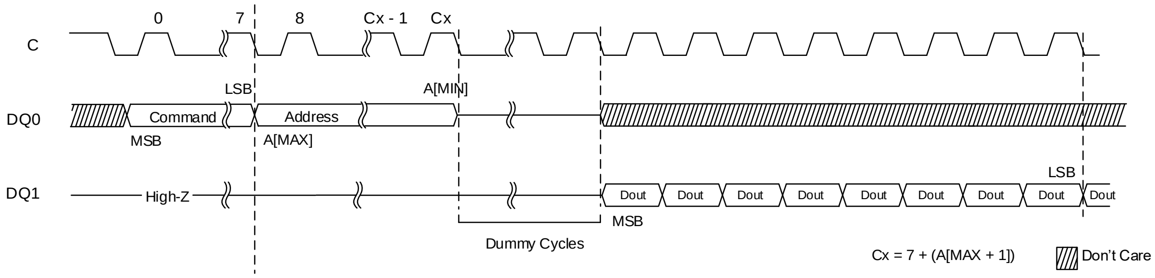
8.14 ONE-TIME PROGRAMMABLE OPERATION

READ OTP ARRAY COMMAND

To initiate READ OTP ARRAY command, S# is driven LOW. The command code is input on DQ0, followed by address bytes and dummy clock cycles. Each address bit is latched in during the rising edge of C. Data is shifted out on DQ1, beginning from the specified address and at a maximum frequency of fC (MAX) on the falling edge of the clock. The address increments automatically to the next address after each byte of data is shifted out. There is no rollover mechanism; therefore, if read continuously, after location 0x40, the device will output invalid data. The operation is terminated by driving S# HIGH at any time during data output.

Figure 8.22 READ OTP Command

Extended



Notes:

1. **Requires 4-bytes of address if device is configured to 4-byte address mode.**
2. **In Octal DDR protocol, command, address, and data-input bits are transmitted on all eight DQ pins in DDR mode, and address is fixed with 4-byte mode.**
3. **S# is not shown.**

PROGRAM OTP ARRAY COMMAND

To initiate PROGRAM OTP ARRAY command, the WRITE ENABLE command must be issued to set the write enable bit to 1; otherwise, the PROGRAM OTP ARRAY command is ignored and flag status register bits are not set. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by address bytes and at least one data byte. Each address bit is latched. The command code is input on DQ0, followed by address bytes and at least one data byte. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is tPOTP. There is no rollover mechanism; therefore, after a maximum of 65 bytes are latched in the subsequent bytes are discarded.

PROGRAM OTP ARRAY programs, at most, 64 bytes to the OTP memory area and one OTP control byte. When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not, and the status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0.

If the operation times out, the write enable latch bit is reset and program fail bit is set to 1. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output.
The OTP control byte (byte 64) is used to permanently lock the OTP memory array.

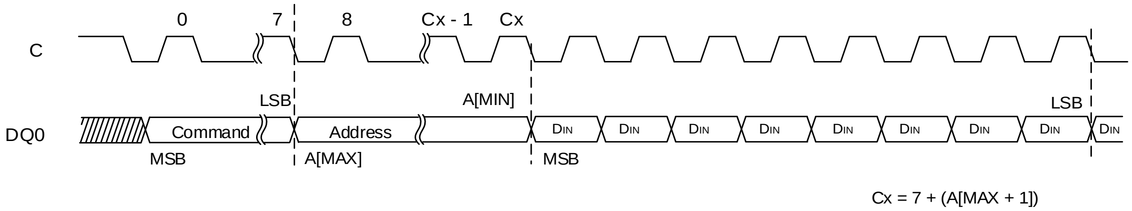
8.15 ONE-TIME PROGRAMMABLE OPERATION

Table 8.15 OTP Control Byte (Byte 64)

Bit	Name	Settings	Description
0	OTP control byte	0 = Locked 1 = Unlocked (Default)	Used to permanently lock the 64-byte OTP array. When bit 0 = 1, the 64-byte OTP array can be programmed. When bit 0 = 0, the 64-byte OTP array is read only. Once bit 0 has been programmed to 0, it can no longer be changed to 1. Program OTP array is ignored, the write enable latch bit remains set, and flag status register bit 1 and 4 are set.

Figure 8.23 PROGRAM OTP Command

Extended



Notes:
1. **Requires 4-bytes of address if device is configured to 4-byte address mode.**
2. **In Octal DDR protocol, command, address, and data-input bits are transmitted on all eight DQ pins in DDR mode, and address is fixed with 4-byte mode.**
3. **S# is not shown.**

8.16 ADDRESS MODE OPERATION

To initiate these commands, S# is driven LOW, and the command is input on DQn.

Table 8.16 ENTER or EXIT 4-BYTE ADDRESS MODE Operations

Operation Name	Description/Conditions
ENTER 4-BYTE ADDRESS MODE (B7h)	The effect of the command is immediate. The default address mode is three bytes, and the device returns to default upon exiting the 4-byte address mode.
EXIT 4-BYTE ADDRESS MODE (E9h)	

Note:

1. **3-byte address mode (Default) or 4-byte address mode in Extended protocol. In Octal DDR protocol, always fixed 4-byte address mode is supported.**

8.17 STATE TABLE

The device can be only one state at a time except for read while program/erase operation. Depending on the state of the device, some operations shown in the table below are allowed (Yes) and others are not (No).
For example, when the device is in standby state, all operations except SUSPEND are allowed in any sector. In the erase suspend state, a PROGRAM operation is allowed in any sector except the one in which an ERASE operation has been suspended.

Table 8.17 Operations Allowed/Disallowed During Device States

Operation	Standby State	Program or Erase State	Subsector Erase Suspend or Program Suspend State	Erase Suspend State	Notes
READ Flash Array	Yes	**Yes[8]/No**	Yes	Yes	1
READ (status/flag status/volatile configuration registers)	Yes	Yes	Yes	Yes	6
PROGRAM	Yes	No	No	Yes/No	2
ERASE (sector/subsector)	Yes	No	No	No	3
WRITE	Yes	No	No	No	4
WRITE	Yes	No	Yes	Yes	5
SUSPEND	No	Yes	No	No	7

Notes:

1. **When issued to a sector or subsector that is simultaneously in an erase suspend state, the READ operation is accepted, but the data output is not guaranteed until erase has completed.**
2. **All PROGRAM operations except PROGRAM OTP Array (42h). In the erase suspend state, a PROGRAM operation is allowed in any sector (Yes) except the sector (No) in which ERASE operation has been suspended.**
3. **Applies to the SECTOR ERASE or SUBSECTOR ERASE operation.**
4. **Applies to the following operations: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM OTP Array, WRITE PROTECTION MANAGEMENT REGISTER, WRITE PASSWORD, PROGRAM SECTOR PPROTECTION and CHIP ERASE.**
5. **Applies to the following operations: WRITE VOLATILE CONFIGURATION REGISTER, WRITE ENABLE, WRITE DISABLE, CLEAR FLAG STATUS REGISTER operation.**
6. **Applies to READ STATUS REGISTER, READ FLAG STATUS REGISTER or READ volatile configuration REGISTER operation.**
7. **Applies to PROGRAM SUSPEND or ERASE SUSPEND operation.**
8. **In an optional device (option L), READ Flash Array operation is allowed in any bank (Yes) except the bank (No) in which PROGRAM/ERASE operation has been in progress (Read While Write Operation).**

8.18 XIP MODE

Execute-in-place (XIP) mode allows the memory to be read by sending an address to the device and then receiving the data on one or eight pins in parallel, depending on the customer requirements. XIP mode offers maximum flexibility to the application, saves instruction overhead, and reduces random access time.

ACTIVATE or TERMINATE XIP Using Volatile Configuration Register

Applications that boot in SPI and must switch to XIP use volatile configuration register. XIP provides faster memory READ operations by requiring only an address to execute, rather than a command code and an address.

To activate XIP requires two steps;

- First, enable XIP by setting volatile configuration register (byte 6).
- Next, drive the XIP confirmation bit to 0 during next FAST READ operation. XIP is then active.

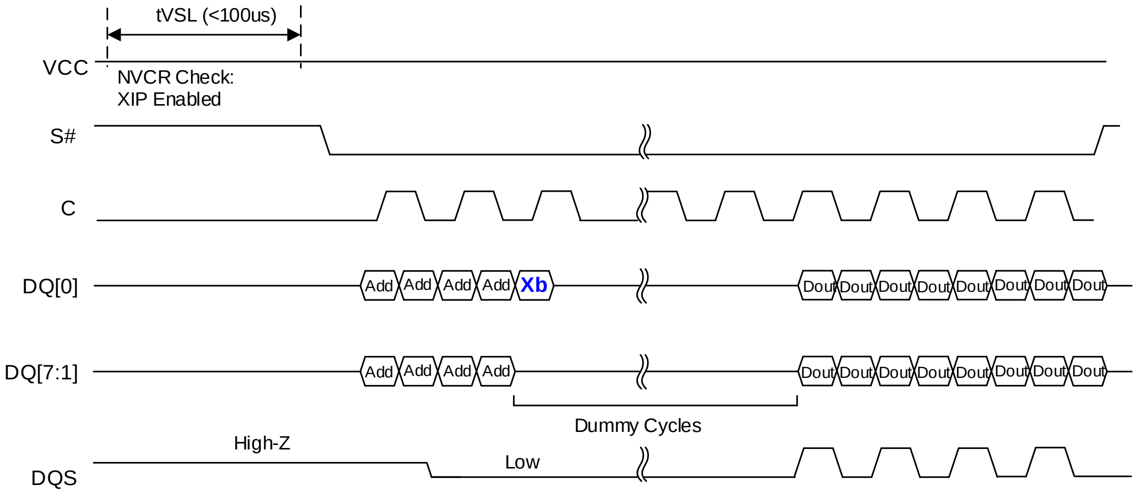
Once in XIP, any Fast Read Operation that occurs after S# is toggled requires only address bits to execute; a Fast Read command code is not necessary, and device operations use the SPI protocol.
XIP is terminated by driving XIP confirmation bit to 1. Then the device automatically resets the XIP volatile configuration register to FFh.

ACTIVATE or TERMINATE XIP Using Nonvolatile Configuration Register

Applications that must boot directly in XIP use nonvolatile configuration register. To enable a device to power-up in XIP using register, set nonvolatile configuration register (byte 6). Settings vary according to protocol, as explained in the Nonvolatile Configuration Register Section. Because the device boots directly in XIP, after the power cycle, no command code is necessary. XIP is terminated by driving XIP confirmation bit to 1.

Figure 8.24 XIP Mode Entered at Power-On

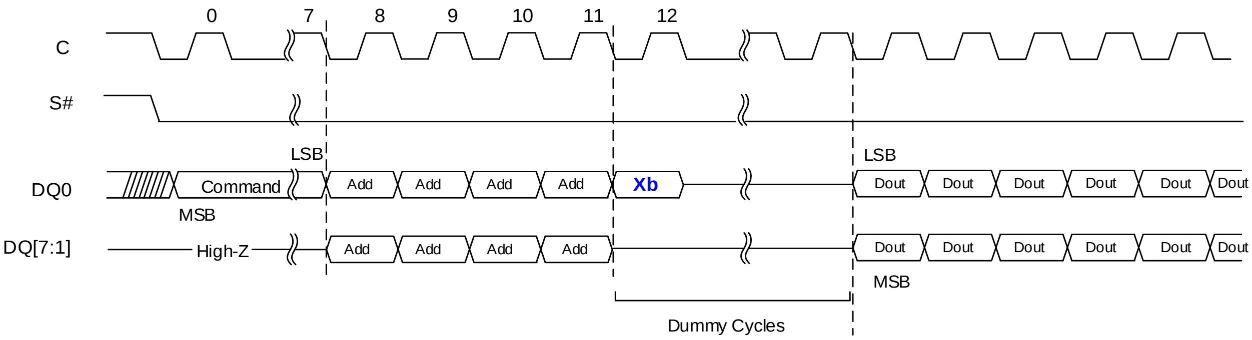
Octal DDR



Notes:
1. **Xb is the XIP confirmation bit and should be set as follows: 0 to keep XIP state; 1 to exit XIP mode and return to standard read mode.**
2. **Example of NVCR. 06h = FEh (8IOFR XIP) in Octal DDR protocol**

Figure 8.25 XIP Mode Entry by Volatile Configuration Register

Extended



Notes:

1. **Xb is the XIP confirmation bit and should be set as follows: 0 to keep XIP state; 1 to exit XIP mode and return to standard read mode.**
2. **Example of NVCR. 06h = FEh (8IOFR XIP) in Extended SPI protocol**

Confirmation Bit Settings Required to Activate or Terminate XIP

The XIP confirmation bit setting activates or terminates XIP after it has been enabled or disabled. This bit is the value on DQ0 during the first dummy clock cycle in the FAST READ operation. In Octal I/O XIP mode, the values of DQ 7:1] during first dummy clock cycle after the address are always “Don’t Care”.

Table 8.18 XIP Confirmation Bit

Bit Value	Description
0	Activates XIP: While this bit is 0, XIP remains activated.
1	Terminates XIP: While this bit is 1, XIP remains terminated and the device returns to SPI.

Table 8.19 Effects of Running XIP in different Protocols

XIP Configuration (NVCR. 06h)	Description
Fast Read (F8h), 8OFR (FDh) in Extended SPI protocol	A LOW pulse on RESET# pin resets XIP and the device to the state it was in previous to the last power-up, as defined by the non-volatile configuration register.
8IOFR (FEh) in Extended SPI protocol	Values of DQ [7:1] during first dummy clock cycles are “Don’t Care”.
Fast Read (F8h), 8OFR (FDh), 8IOFR (FEh) in Octal DDR protocol	

Terminating XIP after a Controller and Memory Reset

The system controller and the device can become out of synchronization if, during the life of the application, the system controller is reset without the device being reset. In such a case, the controller can reset the memory to power-on reset if the memory has reset functionality.

The following sequence causes the controller to set the XIP configuration bit to 1, thereby terminating XIP. However, it does not reset the device or interrupt PROGRAM/ERASE operations that may be in progress. After terminating XIP, the controller must execute RESET ENABLE and RESET MEMORY to implement a software reset and reset the device. It's required to have DQ0 equal to 1 for the situations listed here:

- 3 clock cycles within S# LOW (S# becomes (S# becomes HIGH before 4th clock cycle) +
- 4 clock cycles within S# LOW (S# becomes (S# becomes HIGH before 5th clock cycle) +
- 5 clock cycles within S# LOW (S# becomes (S# becomes HIGH before 6th clock cycle) +
- 25 clock cycles within S# LOW (S# becomes (S# becomes HIGH before 26th clock cycle) +
- 33 clock cycles within S# LOW (S# becomes (S# becomes HIGH before 34th clock cycle) +

8.19 POWER-UP AND POWER-DOWN

Power-Up and Power-Down Requirements

At power-up and power-down, the device must not be selected; that is, S# must follow the voltage applied on Vcc reaches the correct values; V_{CC},min at power-up and V_{SS} at power-down.

To provide device protection and prevent data corruption and inadvertent WRITE operations during power-up, a power-on reset circuit is included. The logic inside the device is held to RESET while V_{CC} is less than the power-on reset threshold voltage shown here; all operations are disabled, and the device does not respond to any instruction. During a standard power-up phase, the device ignores all commands except READ STATUS REGISTER and READ FLAG STATUS REGISTER. These operations can be used to check the memory internal state. After power-up, the device is in standby power mode; the write enable latch bit is reset; the write in progress bits is reset; and the dynamic protection register is configured as (write lock bit, lock down bit) = (0, 0).

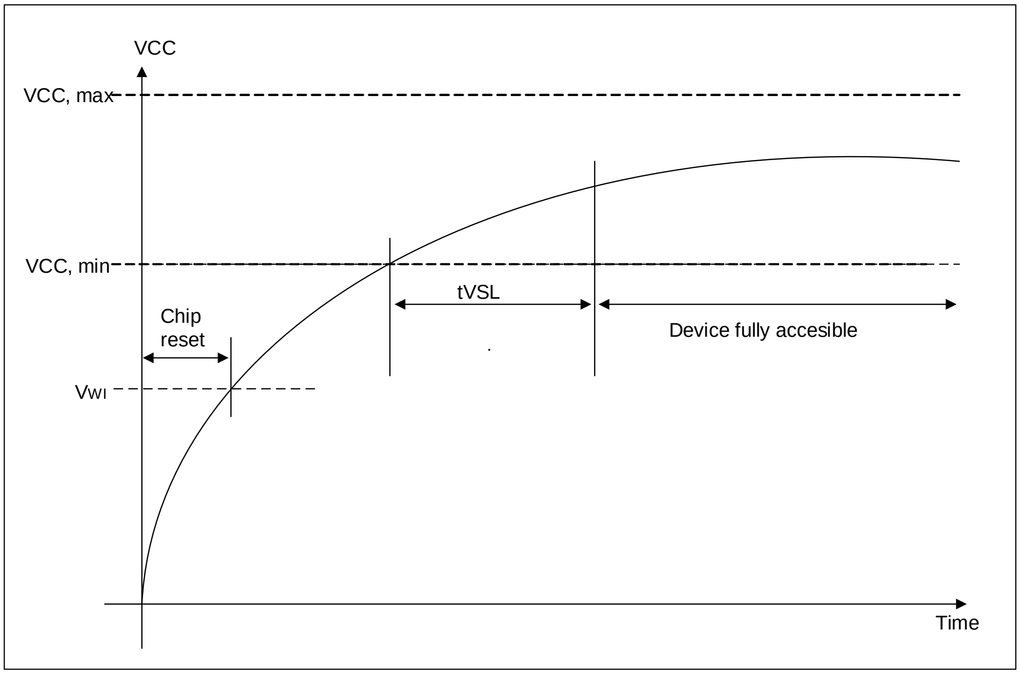
Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitful capacitor (typically 100nF) close to package pins. At power-down, when V_{CC} drops from the operating voltage to below the power-on-reset threshold voltage shown here, all operations are disabled and the device does not respond to any command.

When the operation is in progress, the program or erase controller bit of the status register is set to 0. To obtain the operation status, the flag status register must be polled. When the operation completes, the program or erase controller bit is cleared to 1. The cycle is complete after the flag status register outputs the program or erase controller bit to 1.

Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, data corruption may occur.

V_{PPH} must be applied only when V_{CC} is stable and in the $V_{CC,min}$ to V_{CC}, max voltage range.

Figure 8.26 Power-Up Timing



Notes:

1. **During tVSL period, output strength is default setting and DQS is disabled.**

Table 8.20 Power-Up Timing and V_{WI} Threshold

Symbol	Parameter		Min	Max	Unit	Notes
tVSL	VCC, min to device accessible		300	-	us	1, 2
VWI	Write Inhibit Voltage	IS25LX	-	2.5	V	1
		IS25WX	-	1.5	V	1

Notes:

1. **Parameters listed are characterized only.**
2. **On the first power-up after an event causing a sub-sector ERASE operation interrupt (for example, due to power-loss), the maximum time for tVSL will be up to 4.5ms in case of 4KB subsector erase interrupt and up to 36ms in case of 32KB sub-sector erase interrupt, this accounts for erase recovery embedded operation.**

8.20 DATA LEARNING PATTERN READ OPERATION FOR TRAINING (DLPRD)

The Data Learning Pattern is preamble bits, and it can help host controller to determine the phase shift from clock to data edges so that controller can capture data at the center of the data eye at high frequency operation.

DLPRD function is supported in both Extended SPI mode and Octal DDR mode.

- DLPRD (CDh) in Extended SPI mode: 1S-0-8D operation, 8-bit SDR command is transferred through DQ0 only, and DDR data is transferred through DQ0 to DQ7
- DLPRD (CDh+CDh) in Octal DDR mode: 8D-0-8D, 16-bit DDR command and DDR data are transferred through DQ0 to DQ7.
- **DQS must be always ON during DLPRD operation.**

Note: To place DQS and DQ on the same position with DDR Octal I/O Read or Octal DDR read operation with 32-bit address, dummy cycle of DLPRD = Dummy cycle setting of each operation + 2 clock cycle (Default: 16 cycles + 2 cycles = 18 cycles).

The sequence of issuing DLPRD instruction is: CE# goes low → sending DLPRD instruction → dummy cycles → DLP data out repeatedly until CE# goes high.

Note: DLP data is repeated after beat 7 if CE# remains LOW until CE# goes HIGH.
Beat 7 →beat 6→…beat 0→beat 7→ beat 6→….

DLP pattern is an 8-bit data pattern in Configuration Register (bits [7:0], address; 0Ah), and default values are 01010101.
Predefined pattern can be changed with Configuration Register Write Operation.

Also SSO pattern can be selected when SSOENB bit of Configuration Register (bit [6], address; 0Bh) sets to "1" like below.

Table 8.21 Data Learning Pattern

SSOSEL (bit 6, 0Bh)	**IO Pattern**	**DQ0~DQ2, DQ4~DQ7**	**DQ3**
Bit 6 = 1 (default; SSO disabled)	All 8 DQs are same	0101 0101	0101 0101
Bit 6 = 0 (SSO enabled)	DQ3 is inverted (7 DQs are same)	0101 0101	1010 1010

Figure 8.27 DLPRD Sequence in Extended SPI mode (NVCR. 00h = FFh)

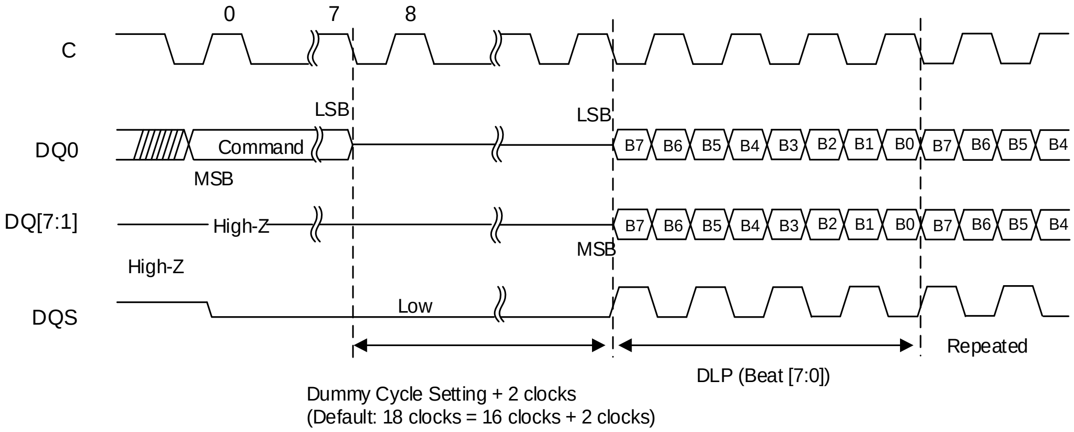
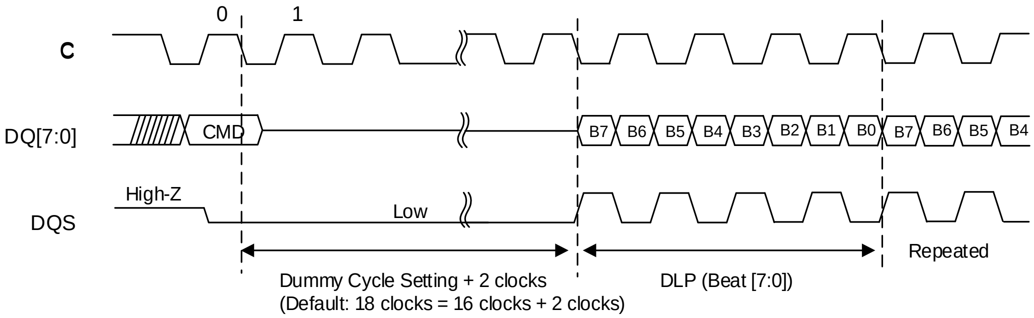


Figure 8.28 DLP READ Sequence in Octal DDR mode.



8.21 ECC OPERATION

ECC (Error Checking and Correcting) is to prevent stored data errors.

The device implemented On-Chip ECC, which can correct 1-bit error and detect 2-bit error per 16-byte chunk. (SEC-DED: Single Error Correction and Double Error Detection)

When ECC is ON, it is recommended that data be programmed in multiple of 16 bytes in predefined 16-byte chunk address using Page Program command instead of single byte or single word programming.

However, partial programming of 16-byte chuck is allowed under the restriction that user cannot program or alter the content of partially programmed chunk without erasing a sector, which includes partially programmed chunk.

Double programming (rewriting without erase), or rewrite partially programmed chunk (alternating of single bit, byte, or word without erasing within 16-byte ECC chunk) is an illegal operation, and automatically aborted. Also bit 7 of address 0Bh of volatile configuration register will be set to 1.

ECC registers show detailed information for error correction activity on the device. The ECC status registers are placed on the Volatile Configuration Register, which include 3-bit ECC status (bit [2:0] in address 0Ch) to identify the error type, 4-bit ECC counter (bit [6:3]and first event chunk address (address 14h~address 17h).
First ECC event for chunk address will be selected by setting of EERRBECC bit of 0Bh.

The Volatile ECC registers values can be reset through either of the following situations:

- CLRERR command (B6h)
- Issuing Software RESET command
- Hardware RESET
- JEDEC Standard In-Band RESET
- Power-up cycle

Table 8.22 16-byte ECC Chunks within a Page (256 byte)

Chunk#	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
16 Bytes	**B0 ~ B15**	**B16 ~ B31**	**B32 ~ B47**	**B48 ~ B63**	**B64 ~ B79**	**B80 ~ B95**	**B96 ~ B127**	**B128 ~ B143**	**B144 ~ B159**	**B160 ~ B175**	**B144 ~ B159**	**B176 ~ B191**	**B192 ~ B207**	**B208 ~ B223**	**B224 ~ B239**	**B240 ~ B255**

8.22 ADDRESS PARITY CHECK AND ARRAY DATA CRC CHECK OPERATION

ADDRESS PARITY

The address parity check function and array data CRC check (1-bit CRC) function are supported at Octal DDR protocol only when access array data.

The WCRCENB bit (bit 3 in Configuration Register [address 0Bh]) can enable both program address parity check function and program data CRC check. Both are **EVEN** parity check.

The RCRCENB bit (bit 7 in Configuration Register [address 0Bh]) can enable both read address parity check function and read data CRC check. Both are also **EVEN** parity check.

For an address parity check operation, the host must input parity check bits (8-bits) on the rising edge of clock after the 4-byte address cycles in Octal DDR mode.

If Parity error during read operation is detected: There is no read data output (output goes to Hi-Z), and **PARSTAT bit (bit [1] of 0Ch in volatile configuration register) will be set to “1”,** CLRERR command (B6h) will clear PARSTAT bit to “0**.**

If Parity error during program operation is detected: program operation is aborted, **PARSTAT bit (bit [1] of 0Ch in volatile configuration register) will be set to “1”,** CLRERR command (B6h) will clear PARSTAT bit to “0**.**
WEL bit remains “1”, and PROGRAM bit (bit [4] of Flag Status Register) will be set to “1”. CLEAR FLAG STATUS REGISTER (50h) command will clear PROGRAM bit to “0.

The address parity bits are calculated by bitwise exclusive-OR of corresponding input pin.
(bit 0 is calculated by addresses on the DQ0 pin; A0, A8, A16, and A24 out of 32 addresses).

ARRAY DATA CRC

The array data CRC check function is a data parity check function in a program or read operation.

When Program CRC is enabled, the program data size must be multiple of CRC chunk size, set by CRCSIZE bits (bits [5:4] of address 0Bh in configuration register), and 8-bit CRC code (data parity bits) should be following program data of CRC chunk size on the rising edge of clock.

If CRC chunk size is set to 16-byte, and total program data size is 32-byte, then host will input 8-bit CRC code on the rising clock edge after 16-byte of programming data. Remaining 16-byte of program data will be input on the next rising edge of clock, and 8-bit CRC code will be followed after the end of program data.

When Read CRC is enabled, the read data size must be multiple of CRC chunk size, too. And 8-bit CRC code (data parity bits) should be following read data of CRC chunk size on the rising edge of clock.

Starting address has to be at CRC chunk boundary.
Otherwise, array data CRC check might result in an error, and program/read operation would be aborted.
The CRC chunk unit is default to set as 16 bytes.

If CRC error is detected due to CRC error or starting address chunk boundary violation, the command will be aborted, CRCSTAT bit (bit [0] of 0Ch in volatile configuration register) will be set to “1”. CLRERR command (B6h) will clear CRCSTAT bit to “0”

Especially, when CRC error is detected during program operation, **WEL bit remains “1”, and PROGRAM bit (bit [4] of Flag Status Register) will be set to “1”. CLEAR FLAG STATUS REGISTER (50h) command will clear PROGRAM bit to “0**.

8-bit CRC code is also calculated by bitwise exclusive-OR of corresponding input pin in the CRC chunk. For example, CRC code bit 0 is calculated by all the bits of DQ0 pin in the CRC chunk.

Figure 8.29 Address Parity and PROGRAM Array Data CRC Timing (S#, C, DQ [7:0])

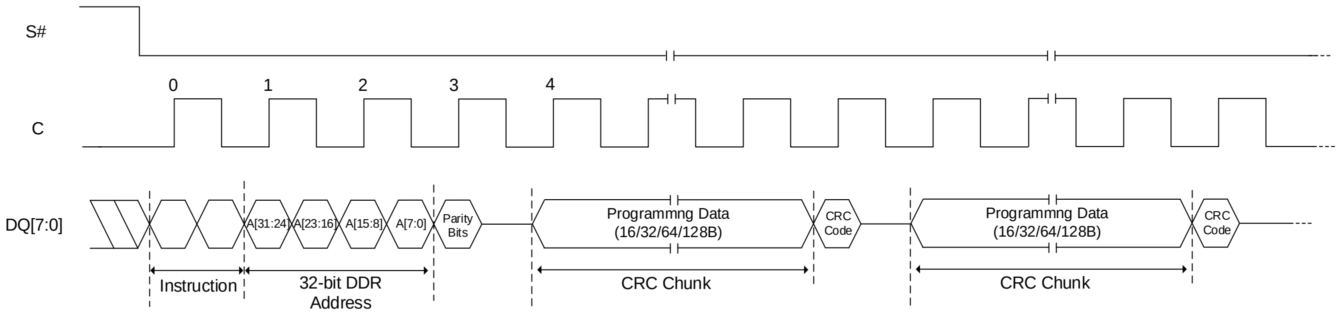
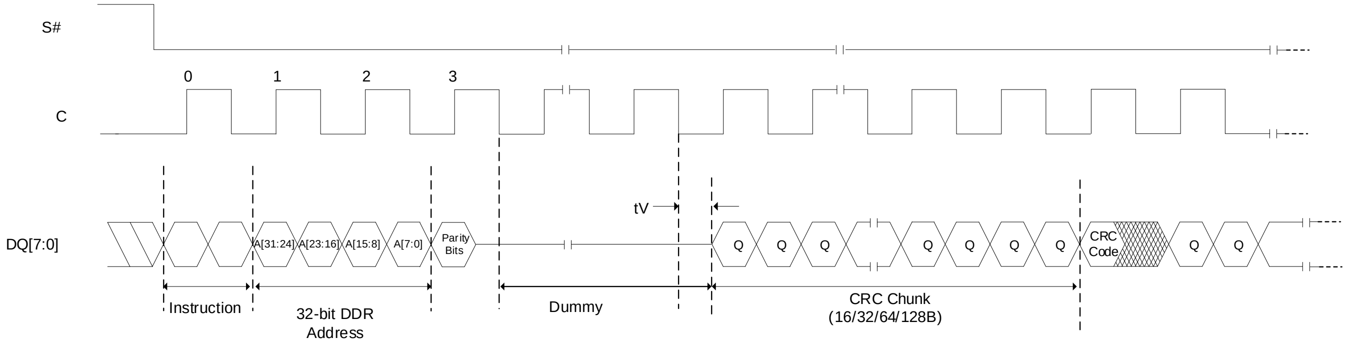


Figure 8.30 Address Parity and Read Array Data CRC Timing (S#, C, DQ [7:0])



8.23 ERR# SIGNAL OPERATION

The ERR# pin is a real time indication signal for the ECC event.
The ERR# pin is designed as an open drain structure.

In normal situation, the ERR# is kept on Hi-Z state. Once ECC event occurs, the ERR# pin will pull LOW and stays LOW until RESET the device or until CLRERR command (B6h) is issued.

When ERR# signal goes LOW after detecting ECC error, especially when 2-bit detection error occurred, ERR# signal must be LOW before the end of ECC chunk read data for host to block wrong read data from the device.

So valid ERR# LOW signal must be within ECC chunk read data (tERR).
tERR is from beginning of ECC chunk read data to ERR# LOW, and is maximum 2 clock cycles.

Symbol	Parameter	Min	Typ	Max	Units
tERR	ERR# Access time from beginning of ECC chunk	-		2	Clock

The user can select ERR# corresponding ECC event type; 1-bit correction or 2-bit detection by setting ERRBECC bit (bit 2 of address 0Bh in configuration register).

ERRBECC bit also selects ECC event type for storage of ECC occurred address location.

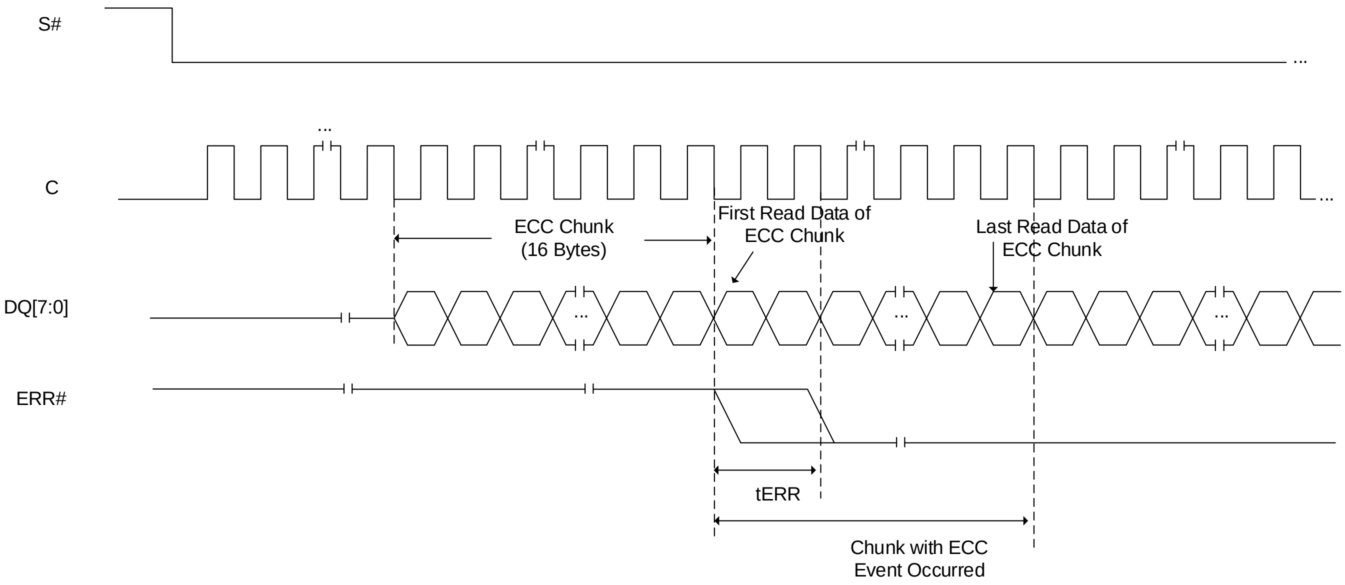
If it is set to “1”,

- ERR# signal reacts only to the 2-bit detection only.
- The address for first 2-bit detection occurred location will be stored on the volatile configuration register (address 10h~0Dh).

To confirm error type (2-bit detection) after ERR# signal goes LOW, host could check ECCSTAT bits (bit [2] of address 0Ch in configuration register).

The ERR# signal goes to high-z state by CLRERR command (B6h), which also clears all volatile register values related Parity error, CRC error and ECC error.

Figure 8.31 ERR# Signal Timing when detecting ECC error



8.24 CLEAR ERRB OPERATION

The CLERRB operation (B6h) disables ERR# signal, which has been LOW to indicate ECC error.

Also it resets ECCSTAT bit, PARSTAT bit, CRCSTAT bit, ECCCOUNTER bits, IPA_ECCB bit, and ECCFCA bits to default state.

Also power-on cycle or Hardware RESET/Software RESET operation will disables ERR# signal, and clears volatile register bits.

8.25 READ WHILE PROGRAM/ERASE OPERATION

The read while program/erase feature allows the host system to read data from any other 3 banks while program or erase operation is in progress at one bank of memory array

The Read while program/erase feature can be used to perform the following:
- Read another bank out of remaining 3 banks of memory array while Erase is in progress in one bank.
- Read another bank out of remaining 3 banks of memory array while Program in progress in one bank.
- At any time, only one bank is available for program/erase operation.

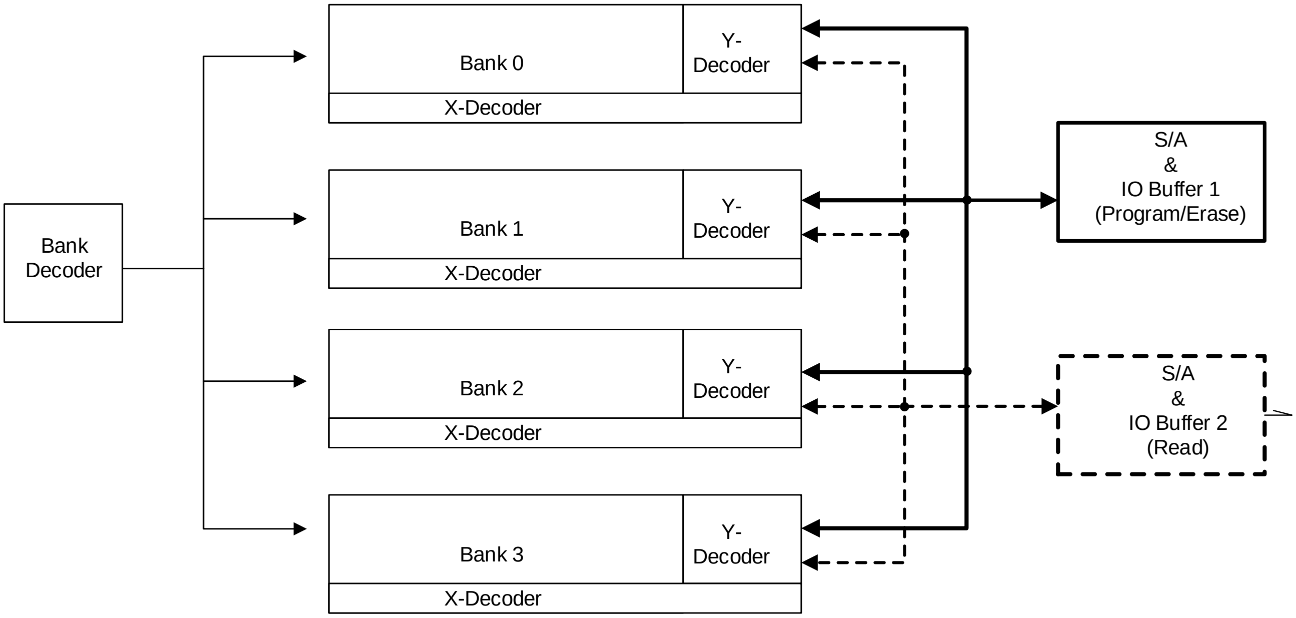
To check which bank is in the middle of program/erase operation, host can check it by reading BANKSTAT bits [bit [2:0] of address 17h]

The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately read array data from remaining bank, with zero latency.

This releases the system from waiting for the completion of program or erase operations or suspend operation.

NOTE: Read while Program/Erase function is supported by optional device (option L) only.

Figure 8.32 Block Diagram while Program/Erase Operation



8.26 PHASE SHIFTED CLOCK FOR CENTER ALIGNED DQS IN OCTAL DDR OPERATION

The device offers an optional feature of PCS (Phase Shifted Clock), which makes no timing relationship between data strobe (DQS) and read data. The feature is provided in certain devices, based on the Ordering Part Number.

When PSC (Phase Shifted Clock) clock is provided, PSC clock will be used as a reference for DQS signal to put DQS signal on the center of read data valid window.

- C is the reference for Read data Q
- PSC is the reference for Data Strobe DQS.
- PSC is supported only with BGA package.

Normally PSC clock is a copy of C clock that is phase shifted 90 degrees. However, other degrees of phase shift between C and PSC may be used by host to optimize DQS position.

PSC is not used for write operation. Also DQS must be enabled for PSC mode.

Below parameters are defined only for PSC mode.

Table 8.23 Timing Parameters in PSC MODE

Symbol	Parameter		Min	Typ	Max	Units
F_{CT}	Clock Frequency for Fast Read in Octal DDR mode	IS25WX (1.8V)			166	MHz
		IS25LX (3.0V)			133	
t_{DQS}	DQS Valid from PSC clock	@ CL = 10pF			6	ns
		@ CL = 15pF			6.5	
		@ CL = 30pF			7	
tskew	Skew between tV and tDQSQ	133MHz (DDR)	-0.5		0.5	ns
		166MHz (DDR)	-0.4		0.4	ns

Note:
1. Optional 128KB block instead of 64KB block is also supported with part number option.

8.27 IN-BAND RESET

The device offers an additional feature of In-Band RESET function, which uses existing SPI signals to initiate a reset operation, which is different from existing software reset/hardware reset (dedicated RESET# pin);

- Existing software reset commands often depend on the Flash being in a particular mode before they are effective. This makes software based reset sequences depend on slave device and mode.
- Dedicated RESET# pin requires additional pin over traditional 8-pins of SPI Flash device. Also it requires 1 more signal for reset operation.

In Band-RESET operation requires 2-signal pins; S# and DQ0.

- S# is driven active low to select the SPI slave. (note1)
- Clock (C) remains stable in either a high or low state. (note 2)
- SI (DQ0) is driven low by the bus master. (note 3)
- S# is driven high while SI (DQ0) is still low. (note 4)
- Repeat the above 4 steps, each time alternating the state of SI (DQ0).
- After the fourth S# pulse, the slave triggers its internal reset. (note 5)

Note 1 This powers up the SPI slave
Note 2 This prevents any confusion with a command, as no command bits are transferred (clocked)
Note 3 No SPI bus slave drives SI (DQ0) during S# low before a transition of clock (C). Slave streaming output active is not allowed until after the first edge of clock (C).
Note 4 The slave captures the state of SI on the rising edge of S#
Note 5 SI (DQ0) is low on the first S#, high on the second, low on the third, high on the fourth (This provides a 5h, unlike random noise)

NOTE:

This reset sequence is not intended to be used at normal power on, but to be used when the device is not responding to the system including Software Reset command. This reset sequence will be operational from any state that the device may be in. During the reset process, the device will ignore any chip select (command). Once the sequence is completed, the device will respond to normal operation.

Figure 8.33 Timing for In-Band RESET Operation

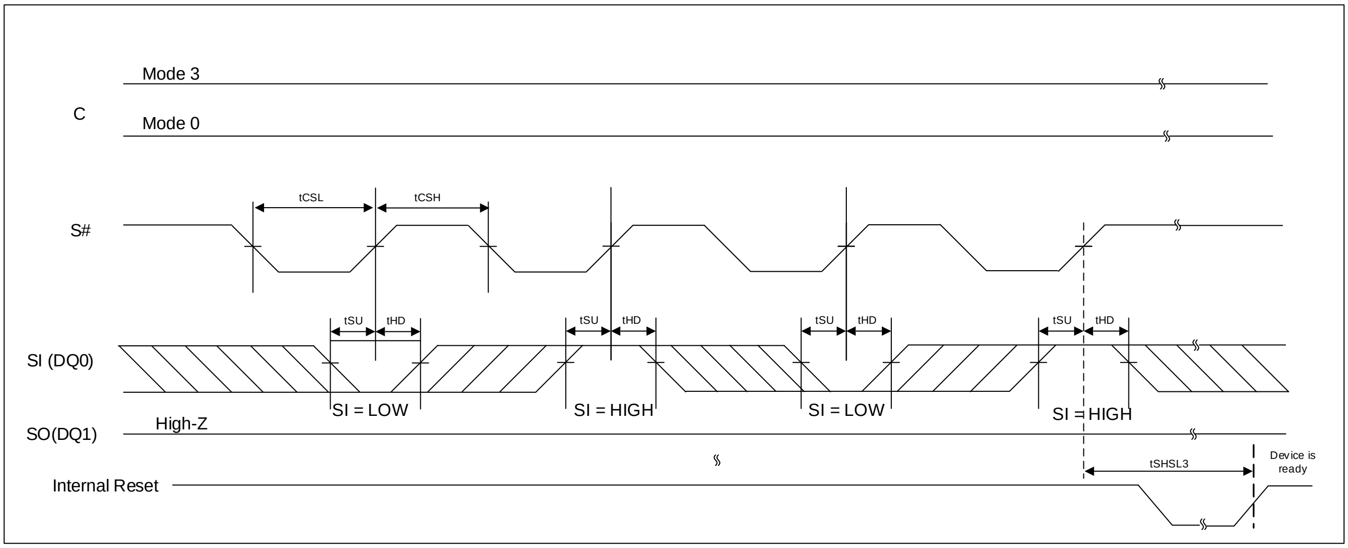


Table 8.24 AC Timings for In Band RESET

Parameter	Min	Max	Units
tCSL	500	-	ns
tCSH	500	-	ns
tSU (Setup Time)	5	-	ns
tHD (Hold Time)	5	-	ns
Reset Recovery Time	tSHSL3 (1)		

Notes:

1. tSHSL3 value is on the Table 9.5

9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Min	Max	Units	Notes
T_{STG}	Storage Temperature		-65	150	°C	
V_{CC}	Supply Voltage	IS25LX	-0.6	4	V	2
		IS25WX	-0.6	2.5		
V_{PP}	Fast Program Voltage		-0.2	10	V	
V_{IO}	I/O voltage with respect to ground		-0.6	V_{CC} + 0.6	V	2
V_{ESD}	Electrostatic Discharge Voltage (human body model)		-2000	2000	V	2, 3

Note:

1. **Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **All specified voltages are with respect to VSS. During infrequent, nonperiodic transitions, the voltage potential between V_{SS} and V_{CC} may undershoot to -2.0V for periods less than 20ns, or overshoot to VCC,max + 2.0V for periods less than 20ns.**
3. **JEDEC Standard JESD22-A114A (C1 = 100pF, R1 = 1500 ohm, R2 = 500 ohm)**

9.1 OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	IS25LX	2.7	3.6	V
		IS25WX	1.7	2.0	
V_{PPH}	Supply Voltage on V_{PP}		8.5	9.5	V
T_A	Ambient Operating Temperature	Extended	-40	105	°C
		Automotive A3	-40	125	°C

9.2 PIN CAPACITANCE (1)

(TA = 25°C, VBIAS=VCC/2, 54MHz)

Symbol	Description	Min	Max	Units
$C_{IN/OUT}$	DQ [7:0], DQS, ERR#	-	5	pF
C_{IN}	Other Input Pin Capacitance: C, W#, RESET#	-	6	pF
$C_{IN/S\#}$	Chip Select (S#)	-	5	pF

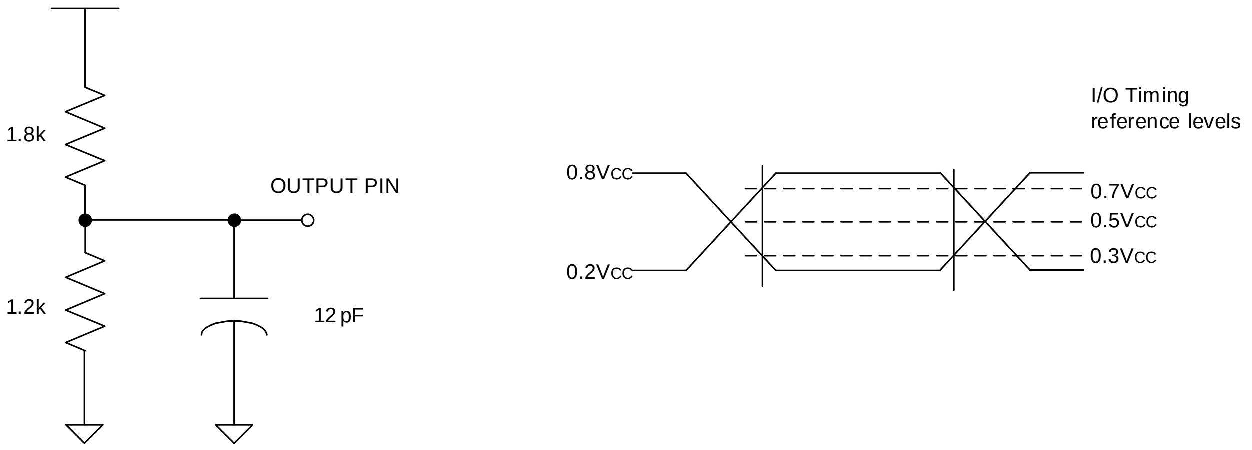
Note: 1. These parameters are not 100% tested and not subject to a production test. They are verified by design and characterization. The capacitance is measured according to JEP147, “PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER” with VCC and VSS applied and all other pins floating (except the pin under test).

9.3 AC TIMING I/O CONDITIONS

Symbol	Parameter		Min	Max	Units
CL(1)	Load Capacitance		-	12	pF
TR,TF	Input Rise and Fall Times	IS25LX		1.5	ns
		IS25WX		1.2	
V_T	Clock Reference Voltage		0.5V_{CC}		V
VIN	Input Pulse Voltages		0.2V_{CC} to 0.8V_{CC}		V
VREFI	Input Timing Reference Voltages		0.3V_{CC} to 0.7V_{CC}		V
VREFO	Output Timing Reference Voltages		0.5V_{CC}		V

Note: 1. Output Buffers are configurable by user, and default value is 50ohm.

Figure 9.1 Output test load & AC measurement I/O Waveform



9.4 DC CURRENT CHARACTERISTICS AND OPERATING CONDITIONS

Table 9.1 DC Current Characteristics and Operating Conditions

Parameter	Symbol	Test Conditions			Typ $^{(1)}$	Max	Units	Notes
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}				±2	µA	
Output Leakage Current	I_{LO}	V_{IN} = 0V to V_{CC}				±2	µA	
Standby Current	I_{CC1}	S# =RESET# = V_{CC}, V_{IN} = V_{CC} or V_{SS}	IS25LX	105°C	10	90	µA	2
				125°C		140	µA	
			IS25WX	105°C	6	90	µA	
				125°C		140	µA	
Deep power down current	I_{CC2}	S# =RESET# = V_{CC}, V_{IN} = V_{CC} or V_{SS}	IS25LX	105°C	7.5	35	µA	3
				125°C		70	µA	
			IS25WX	105°C	1	35	µA	
				125°C		70	µA	
Operating Current (FAST READ EXTENDED I/O)	I_{CC3}	C = 0.1VCC/0.9VCC at 54MHz, DQ1 = Open			12	16	mA	4
		C = 0.1VCC/0.9VCC at 133MHz, DQ1 = Open			14	20	mA	
Operating Current (Octal SDR command)		C = 0.1VCC/0.9VCC at 166MHz, DQ = Open			20	60	mA	
Operating Current (Octal DDR command)		C = 0.1VCC/0.9VCC at 166MHz, DQ = Open			28	66	mA	
		C = 0.1VCC/0.9VCC at 200MHz $^{(6)}$, DQ = Open			33	70	mA	
Operating Current (PROGRAM Operations)	I_{CC4}	S# = V_{CC}			40	60	mA	5
Operating Current (WRITE Operations)	I_{CC5}	S# = V_{CC}			16	45	mA	
Operating Current (ERASE Operations)	I_{CC6}	S# = V_{CC}			40	60	mA	

Notes:
1. Typical values are at VCC (1.8V/3.0V); VI/O = 0V/V_{CC}; TA=25°C
2. Standby current is an average calculated 5 us after S# de-assertion and completion of any internal operation.
3. Deep power-down current is an average calculated during a 5ms time interval 100us after completion of any internal operation.
4. Read current is an average calculated during a 1KB continuous READ operation without load, in a checker-board pattern.
5. Program current is an average measured over a 256-byte data PROGRAM operation.
6. Call Factory for 200MHz

Table 9.2 DC Current Characteristics and Operating Conditions

Parameter	Symbol	Conditions	Min	Max	Units
Input Low voltage (DC)	V_{IL}	-	-0.3	$0.3V_{CC}$	V
Input Low voltage (AC)		-	-0.3	$0.2V_{CC}$	V
Input High voltage (DC)	V_{IH}	-	$0.7V_{CC}$	$V_{CC} + 0.3$	V
Input High voltage (AC)		-	$0.8V_{CC}$	$V_{CC} + 0.3$	V
Output Low voltage	V_{OL}	I_{OL} = 1.6mA	-	0.15 x V_{CC}	V
Output High voltage	V_{OH}	I_{OH} = -100uA	0.85 x V_{CC}	-	V

Note:
1. V_{IL} can undershoot to -1.0V for periods less than 2ns; V_{IH} can overshoot to V_{CC} + max + 1.0V for periods less than 2ns.

9.5 AC CHARACTERISTICS

Table 9.3.1 AC Characteristics and Operating Conditions for IS25WX (VCC = 1.7V to 2.0V, DDR=166MHz)

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Clock frequency for all commands other than READ (03h)	fC	SDR	DC	-	166	MHz	10
		DDR	DC	-	166		
Clock frequency for READ (03h)	tR	SDR	DC	-	54	MHz	
Clock HIGH time	tCH	SDR/DDR	2.7	-	-	ns	2
Clock LOW time	tCL	SDR/DDR	2.7	-	-	ns	2
Clock rise time (peak-to-peak)	tCLCH	SDR/DDR	1/1.2	-	-	V/ns	3, 4
Clock fall time (peak-to-peak)	tCHCL	SDR/DDR	1/1.2	-	-	V/ns	3, 4
S# active setup time (relative to clock)	tSLCH	SDR/DDR	2.25	-	-	ns	
S# Not active hold time (relative to clock)	tCHSL	SDR/DDR	2	-	-	ns	
Data in setup time	tDVCH	SDR/DDR	1.8/0.7	-	-	ns	
	tDVCL	DDR only	0.7	-	-	ns	
Data in hold time	tCHDX	SDR/DDR	1.8/0.7	-	-	ns	
	tCLDX	DDR only	0.7	-	-	ns	
S# active hold time (relative to clock)	tCHSH	SDR	2	-	-	ns	
	tCLSH	DDR	2			ns	
S# Not active setup time (relative to clock)	tSHCH	SDR/DDR	2	-	-	ns	
S# deselect time after a READ command	tSHSL1	SDR/DDR	12	-	-	ns	
S# deselect time after a nonREAD command	tSHSL2	SDR/DDR	50	-	-	ns	
Output disable time	SHQZ	SDR/DDR	-	-	6	ns	3
Data Valid Window	tDVW	DDR	1.3	-	-	ns	
Clock Low to output valid (Cload=12pF)	tCLQV	SDR/DDR	-	-	6	ns	5
Clock High to output valid (Cload=12pF)	tCHQV	DDR	-	-	6	ns	5
Output hold skew	tQHS	DDR	-	-	0.6	ns	
DQS to DQ skew	tDQSQ	DDR	**-**	**-**	0.5	ns	
DQS low after S# low	tSLQSL	DDR	-	-	10	ns	6
S# to DQS High-Z	tSHQSZ	DDR	-	-	8	ns	
Output hold time	tCLQX	SDR/DDR	1.3	-	-	ns	5
	tCHQX	DDR only	1.3	-	-	ns	5

AC Characteristics and Operating Conditions (Continued)

Parameter		Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Write protect setup time		tWHSL	SDR/DDR	20	-	-	ns	7
Enhanced V_{PPH} HIGH to S# LOW		tVPPHSL	SDR/DDR	200	-	-	ns	7
S# HIGH to deep power-down		tDP	SDR/DDR	3	-	-	us	
S# HIGH to standby mode (DPD exit time)		tRDP	SDR/DDR	30	-	-	us	
WRITE STATUS REGISTER cycle time		tW	SDR/DDR	-	1.3	15	ms	
WRITE NONVOLATILE CONFIGURATION REGISTER cycle time		tWNVCR	SDR/DDR	-	0.2	1	s	
WRITE PROTECTION MANAGEMENT REGISTER timing		tPPMR	SDR/DDR	-	0.1	0.5	ms	
Nonvolatile sector lock time		tPPBP	SDR/DDR	-	0.1	2.8	ms	
Program ASP Register		tASSP	SDR/DDR	-	0.1	0.5	ms	
Program password		tPASSP	SDR/DDR	-	0.2	0.8	ms	
Erase nonvolatile sector lock array		tPPBE	SDR/DDR	-	0.2	1	s	
Page program time (256 bytes)		tPP	SDR/DDR	-	0.15	1.8	ms	8
Page program time when Vpp = VPPH (256 bytes)		tPP	SDR/DDR	-	0.08	1.8	ms	8
Program OTP cycle time (64 bytes)		tOTP	SDR/DDR	-	0.2	0.8	ms	
Sector Erase time	128KB	tSE	SDR/DDR	-	0.28	1	s	
	64KB (1)			-	0.15	1		
Subsector Erase time (4KB)		tSE4K	SDR/DDR	-	25	400	ms	
Subsector Erase time (32KB)		tSE32K	SDR/DDR	-	0.13	1	s	
Chip Erase time	64Mb	tBE	SDR/DDR	-	18	45	s	
	32Mb			-	8	24	s	

Notes:
1. Typical values given for TA=25°C
2. tCH + tCL must add up to 1/fC.
3. Value guaranteed by characterization; not 100% tested.
4. Expressed as a slew-rate
5. **The specification only applies when DQS is disabled.**
6. DQS will be driven after S# LOW.
7. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
8. Typical value is applied for pattern: 50% “0” and 50% “1”
9. Maximum frequency is 133MHz for A5h (SFDP Read), 9Eh/9Fh (Read ID), E2h (Read Nonvolatile Lock Bits), 4Bh (Read OTP Array) operation.
10. Maximum frequency is 133MHz for 27h (Read Password) in Extended SPI mode.

Table 9.3.2 AC Characteristics and Operating Conditions for IS25WX (VCC = 1.7V to 2.0V, DDR=200MHz (11))

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Clock frequency for all commands other than READ (03h)	fC	SDR	DC	-	166	MHz	10
		DDR	DC	-	200		
Clock frequency for READ (03h)	tR	SDR	DC	-	54	MHz	
Clock HIGH time	tCH	SDR	2.7	-	-	ns	2
		DDR	2.25	-	-		
Clock LOW time	tCL	SDR	2.7	-	-	ns	2
		DDR	2.25	-	-		
Clock rise time (peak-to-peak)	tCLCH	SDR/DDR	1/1.2	-	-	V/ns	3, 4
Clock fall time (peak-to-peak)	tCHCL	SDR/DDR	1/1.2	-	-	V/ns	3, 4
S# active setup time (relative to clock)	tSLCH	SDR/DDR	2.25	-	-	ns	
S# Not active hold time (relative to clock)	tCHSL	SDR/DDR	2	-	-	ns	
Data in setup time	tDVCH	SDR/DDR	1.8/0.6	-	-	ns	
	tDVCL	DDR only	0.6	-	-	ns	
Data in hold time	tCHDX	SDR/DDR	1.8/0.6	-	-	ns	
	tCLDX	DDR only	0.6	-	-	ns	
S# active hold time (relative to clock)	tCHSH	SDR	2	-	-	ns	
	tCLSH	DDR	2			ns	
S# Not active setup time (relative to clock)	tSHCH	SDR/DDR	2	-	-	ns	
S# deselect time after a READ command	tSHSL1	SDR/DDR	12	-	-	ns	
S# deselect time after a nonREAD command	tSHSL2	SDR/DDR	50	-	-	ns	
Output disable time	SHQZ	SDR/DDR	-	-	6	ns	3
Data Valid Window	tDVW	DDR	1.3	-	-	ns	
Clock Low to output valid (Cload=12pF)	tCLQV	SDR/DDR	-	-	6	ns	5
Clock High to output valid (Cload=12pF)	tCHQV	DDR	-	-	6	ns	5
Output hold skew	tQHS	DDR	-	-	0.5	ns	
DQS to DQ skew	tDQSQ	DDR	-	-	0.4	ns	
DQS low after S# low	tSLQSL	DDR	-	-	10	ns	6
S# to DQS High-Z	tSHQSZ	DDR	-	-	8	ns	
Output hold time	tCLQX	SDR/DDR	1.3	-	-	ns	5
	tCHQX	DDR only	1.3	-	-	ns	5

AC Characteristics and Operating Conditions (Continued)

Parameter		Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Write protect setup time		tWHSL	SDR/DDR	20	-	-	ns	7
Enhanced V_{PPH} HIGH to S# LOW		tVPPHSL	SDR/DDR	200	-	-	ns	7
S# HIGH to deep power-down		tDP	SDR/DDR	3	-	-	us	
S# HIGH to standby mode (DPD exit time)		tRDP	SDR/DDR	30	-	-	us	
WRITE STATUS REGISTER cycle time		tW	SDR/DDR	-	1.3	15	ms	
WRITE NONVOLATILE CONFIGURATION REGISTER cycle time		tWNVCR	SDR/DDR	-	0.2	1	s	
WRITE PROTECTION MANAGEMENT REGISTER timing		tPPMR	SDR/DDR	-	0.1	0.5	ms	
Nonvolatile sector lock time		tPPBP	SDR/DDR	-	0.1	2.8	ms	
Program ASP Register		tASSP	SDR/DDR	-	0.1	0.5	ms	
Program password		tPASSP	SDR/DDR	-	0.2	0.8	ms	
Erase nonvolatile sector lock array		tPPBE	SDR/DDR	-	0.2	1	s	
Page program time (256 bytes)		tPP	SDR/DDR	-	0.15	1.8	ms	8
Page program time when Vpp = VPPH (256 bytes)		tPP	SDR/DDR	-	0.08	1.8	ms	8
Program OTP cycle time (64 bytes)		tOTP	SDR/DDR	-	0.2	0.8	ms	
Sector Erase time	128KB	tSE	SDR/DDR	-	0.28	1	s	
	64KB (1)			-	0.15	1		
Subsector Erase time (4KB)		tSE4K	SDR/DDR	-	25	400	ms	
Subsector Erase time (32KB)		tSE32K	SDR/DDR	-	0.13	1	s	
Chip Erase time	64Mb	tBE	SDR/DDR	-	18	45	s	
	32Mb			-	8	24	s	

Notes:

1. Typical values given for TA=25°C
2. tCH + tCL must add up to 1/fC.
3. Value guaranteed by characterization; not 100% tested.
4. Expressed as a slew-rate
5. **The specification only applies when DQS is disabled.**
6. DQS will be driven after S# LOW.
7. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
8. Typical value is applied for pattern: 50% “0” and 50% “1”
9. Maximum frequency is 133MHz for A5h (SFDP Read), 9Eh/9Fh (Read ID), E2h (Read Nonvolatile Lock Bits), 4Bh (Read OTP Array) operation.
10. Maximum frequency is 133MHz for 27h (Read Password) in Extended SPI mode
11. **Call Factory for 200MHz**

Table 9.4 AC Characteristics and Operating Conditions for IS25LX (VCC = 2.7V to 3.6V)

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Clock frequency for all commands other than READ (03h)	fC	SDR	DC	-	133	MHz	
		DDR	DC	-	133		
Clock frequency for READ (03h)	tR	SDR	DC	-	54	MHz	
Clock HIGH time	tCH	SDR	3.375	-	4.125	ns	2
		DDR	3.375	-	4.125		
Clock LOW time	tCL	SDR	3.375	-	4.125	ns	2
		DDR	3.375	-	4.125		
Clock rise time (peak-to-peak)	tCLCH	SDR/DDR	1.3/1.1	-	-	V/ns	3, 4
Clock fall time (peak-to-peak)	tCHCL	SDR/DDR	1.3/1.1	-	-	V/ns	3, 4
S# active setup time (relative to clock)	tSLCH	SDR/DDR	3.375	-	-	ns	
S# Not active hold time (relative to clock)	tCHSL	SDR/DDR	2	-	-	ns	
Data in setup time	tDVCH	SDR/DDR	1.8/0.7	-	-	ns	
	tDVCL	DDR only	0.7	-	-	ns	
Data in hold time	tCHDX	SDR/DDR	1.8/0.7	-	-	ns	
	tCLDX	DDR only	0.7	-	-	ns	
S# active hold time (relative to clock)	tCHSH	SDR	2	-	-	ns	
	tCLSH	DDR	2			ns	
S# Not active setup time (relative to clock)	tSHCH	SDR	3.375	-	-	ns	
		DDR	6.75			ns	
S# deselect time after a READ command	tSHSL1	SDR/DDR	12	-	-	ns	
S# deselect time after a nonREAD command	tSHSL2	SDR/DDR	50	-	-	ns	
Output disable time	SHQZ	SDR/DDR	-	-	6	ns	3
Data Valid Window	tDVW	DDR	2	-	-	ns	
Clock Low to output valid (Cload=12pF)	tCLQV	SDR/DDR	-	-	6	ns	5
Clock High to output valid (Cload=12pF)	tCHQV	DDR	-	-	6	ns	5
Output hold skew	tQHS	DDR	-	-	0.8	ns	
DQS to DQ skew	tDQSQ	DDR	-	-	0.6	ns	
DQS low after S# low	tSLQSL	DDR	-	-	10	ns	6
S# to DQS High-Z	tSHQSZ	DDR	-	-	8	ns	
Output hold time	tCLQX	SDR/DDR	2	-	-	ns	5
	tCHQX	DDR only	2	-	-	ns	5

AC Characteristics and Operating Conditions (Continued)

Parameter		Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Write protect setup time		tWHSL	SDR/DDR	20	-	-	ns	7
Enhanced V_{PPH} HIGH to S# LOW		tVPPHSL	SDR/DDR	200	-	-	ns	7
S# HIGH to deep power-down		tDP	SDR/DDR	3	-	-	us	
S# HIGH to standby mode (DPD exit time)		tRDP	SDR/DDR	30	-	-	us	
WRITE STATUS REGISTER cycle time		tW	SDR/DDR	-	1.3	15	ms	
WRITE NONVOLATILE CONFIGURATION REGISTER cycle time		tWNVCR	SDR/DDR	-	0.2	1	s	
WRITE PROTECTION MANAGEMENT REGISTER timing		tPPMR	SDR/DDR	-	0.1	0.5	ms	
Nonvolatile sector lock time		tPPBP	SDR/DDR	-	0.1	2.8	ms	
Program ASP Register		tASSP	SDR/DDR	-	0.1	0.5	ms	
Program password		tPASSP	SDR/DDR	-	0.2	0.8	ms	
Erase nonvolatile sector lock array		tPPBE	SDR/DDR	-	0.2	1	s	
Page program time (256 bytes)		tPP	SDR/DDR	-	0.15	1.8	ms	8
Page program time when Vpp = VPPH (256 bytes)		tPP	SDR/DDR	-	0.08	1.8	ms	8
Program OTP cycle time (64 bytes)		tOTP	SDR/DDR	-	0.2	0.8	ms	
Sector Erase time	128KB	tSE	SDR/DDR	-	0.28	1	s	
	64KB (1)			-	0.15	1		
Subsector Erase time (4KB)		tSE4K	SDR/DDR	-	25	400	ms	
Subsector Erase time (32KB)		tSE32K	SDR/DDR	-	0.13	1	s	
Chip Erase time	64Mb	tBE	SDR/DDR	-	18	45	s	
	32Mb			-	8	24	s	

Notes:
1. Typical values given for TA=25°C
2. tCH + tCL must add up to 1/fC.
3. Value guaranteed by characterization; not 100% tested.
4. Expressed as a slew-rate
5. **The specification only applies when DQS is disabled.**
6. DQS will be driven after S# LOW.
7. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
8. Typical value is applied for pattern: 50% “0” and 50% “1”
9. Maximum frequency of A5h (SFDP Read) operation is 100MHz.

AC Reset Specifications

Table 9.5 AC Reset Recovery Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reset pulse width	**tRLRH**		100	-	-	ns
Chip select high to reset high	**tSHRH**	Chip must be deselected before reset is de-asserted	10	-	-	ns
Reset high to chip select low	**tRHSL**		40	-	-	ns
Hardware Reset recovery time	**tRHSL1**	Device deselected (S# HIGH) and is in standby mode	-	-	5	us
		Any READ operations, PROGRAM/ERAE SUSPEND operation, or any WRITE operation to volatile registers are in progress	-	-	5	us
		Any device array PROGRAM, PROGRAM RESUME, PROGRAM OTP, Chip Erase operation, and NONVOLATILE SECTOR LOCK operations are in progress	-	-	30	us
		While an ERASE NONVOLATILE SECTOR LOCK ARRAY operation is in progress	-	tPPBE	-	ms
		While a WRITE STATUS REGISTER operation is in progress	-	tW	-	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	-	tWNVCR	-	ms
		SECTOR ERASE/SUBSECTOR ERASE operation or SECTOR ERASE/SUBSECTOR ERASE RESUME operation is in progress	-	tSE/tSSE	-	s
		Device in deep power-down mode	-	tRDP	-	ms
		While ADVANCED SECTOR PROTECTION PROGRAM operation is in progress	-	tASSP	-	ms
		While PASSWORD PROTECTION PROGRAM operation is in progress	-	tPASSP	-	ms
		While PASSWORD PROTECTION PROGRAM operation is in progress	-	tPASSP	-	ms

Table 9.5 AC Reset Recovery Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Software Reset recovery time/ In-Band Reset recovery time	**tSHSL3**	Device deselected (S# HIGH) and is in standby mode	-	-	5	us
		PROGRAM/ERAE SUSPEND operation is in progress	-	-	5	us
		Any device array PROGRAM, PROGRAM RESUME, PROGRAM OTP, Chip Erase operation, and NONVOLATILE SECTOR LOCK operations are in progress	-	-	30	us
		While an ERASE NONVOLATILE SECTOR LOCK ARRAY operation is in progress	-	tPPBE	-	ms
		While a WRITE STATUS REGISTER operation is in progress	-	tW	-	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	-	tWNVCR	-	ms
		SECTOR ERASE/SUBSECTOR ERASE operation or SECTOR ERASE/SUBSECTOR ERASE RESUME operation is in progress	-	tSE/tSSE	-	s
		Device in deep power-down mode	-	tRDP	-	ms
		While ADVANCED SECTOR PROTECTION PROGRAM operation is in progress	-	tASSP	-	ms
		While PASSWORD PROTECTION PROGRAM operation is in progress	-	tPASSP	-	ms

Notes: 1. Values are guaranteed by characterization; not 100% tested.
2. The device reset is possible but not guaranteed if tRLRH < 100ns.

Figure 9.2 Hardware Reset AC Timing

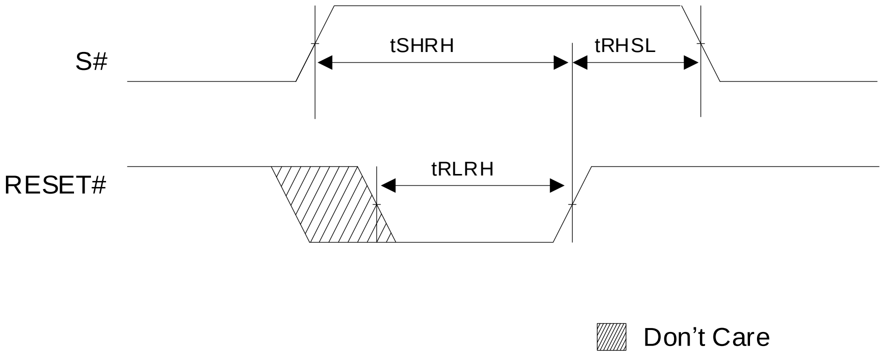


Figure 9.3 SERIAL INPUT TIMING

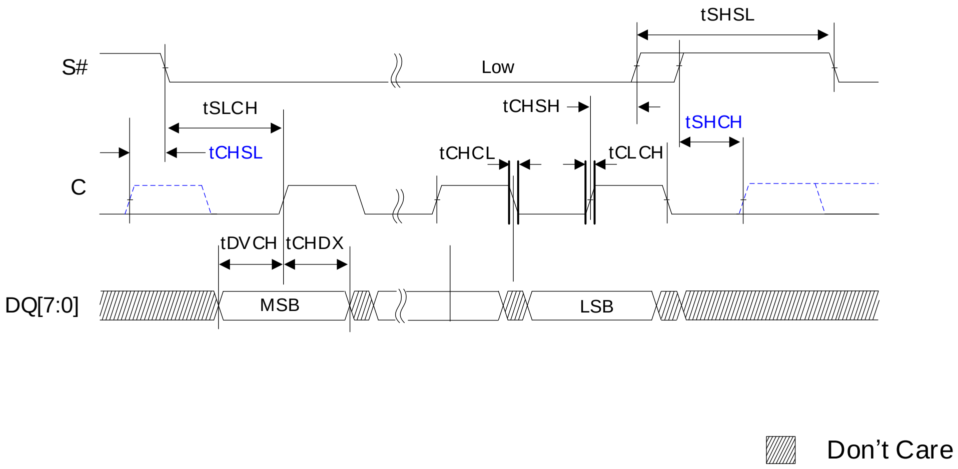


Figure 9.4 SERIAL INPUT TIMING - DDR

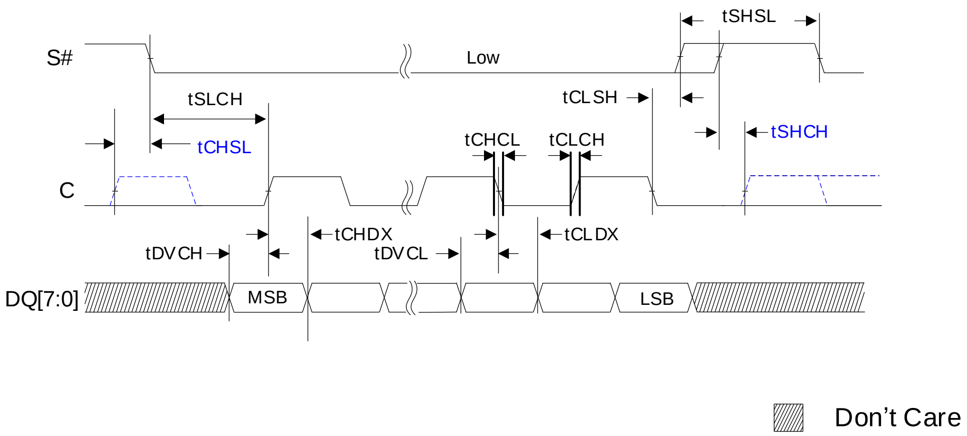


Figure 9.5 Write Protect Setup and Hold During WRITE STATUS REGISTER Operation (SRWD = 1)

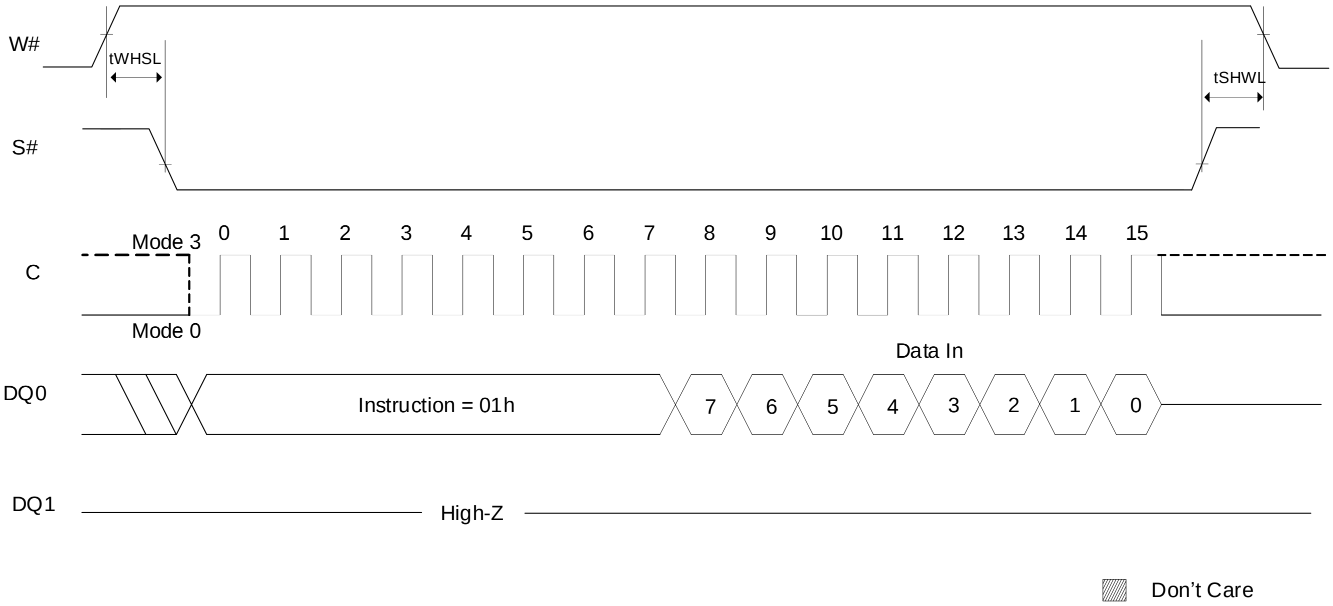


Figure 9.6 Output Timing - SDR

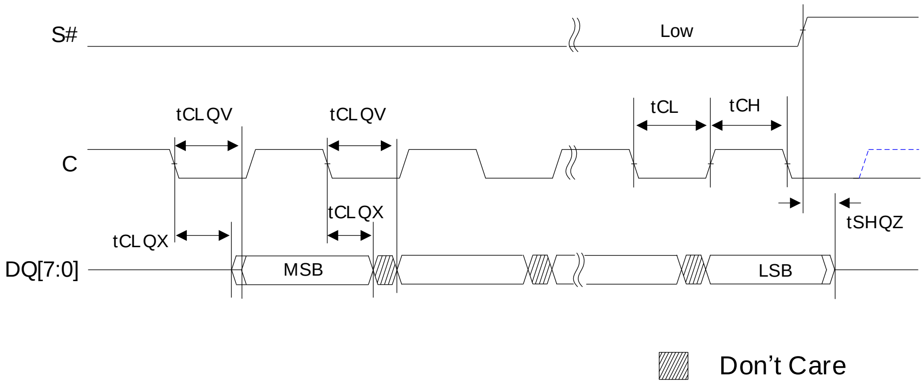


Figure 9.7 Output Timing - DDR

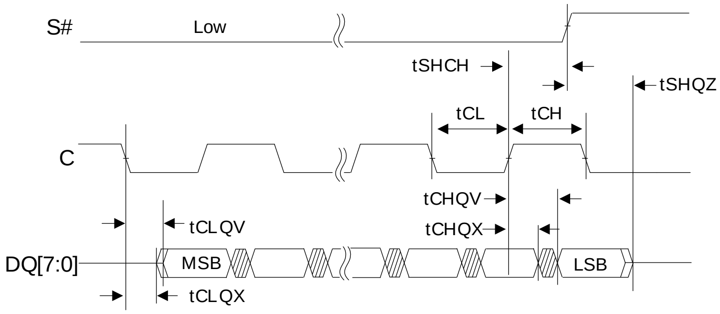
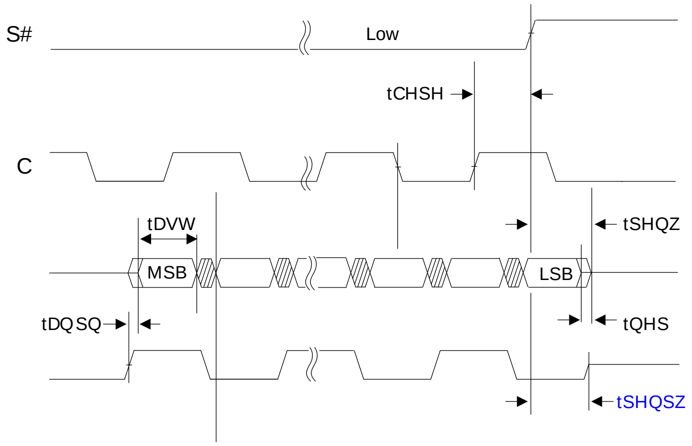


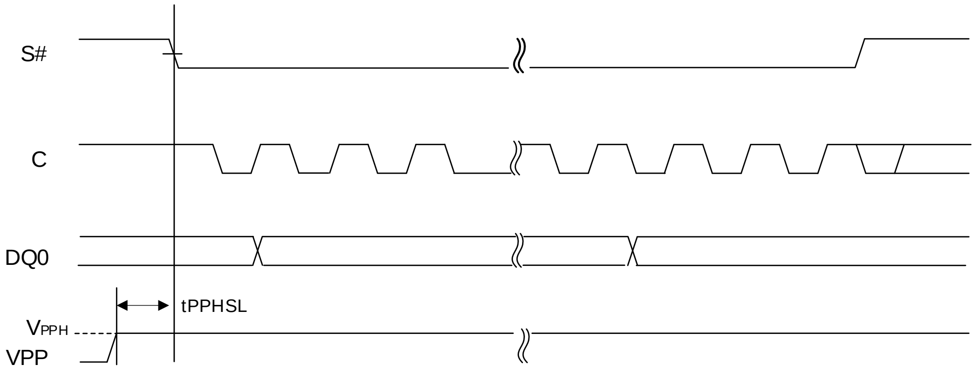
Figure 9.8 Output Timing – DDR with DQS



Note:

1. **The device will be de-selected while clock is HIGH to get even counts of output data. Next DQ (or DQS) output could be observed if clock edge is received before S# goes HIGH.**

Figure 9.9 V_{PPH} Timing



9.6 PROGRAM/ ERASE SUSPEND/RESUME SPECIFICATIONS

Table 9.6 Program/ Erase Suspend/Resume Specifications

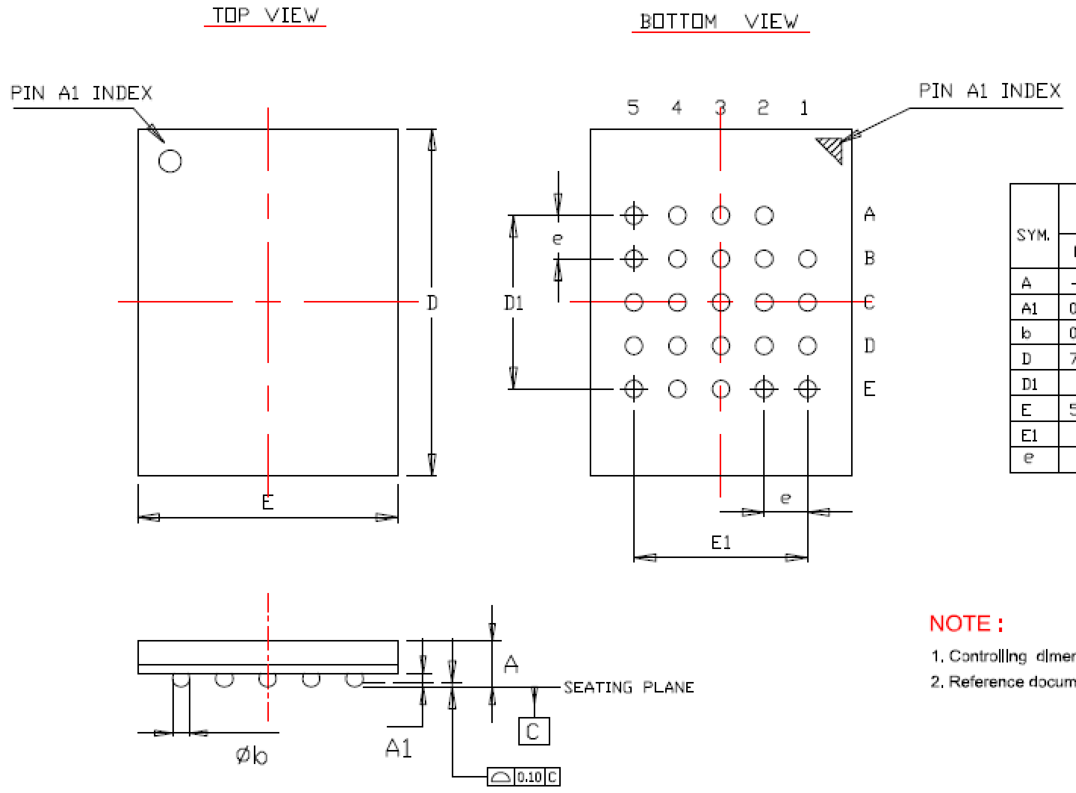
Parameter	Condition	Typ	Max	Units	Notes
Erase to suspend	Sector erase or erase resume to erase suspend	150	-	us	1
Program to suspend	Program resume to program suspend	5	-	us	1
Subsector erase to suspend	Subsector erase or subsector erase resume to erase suspend	50	-	us	1
Suspend Latency	Program	7	25	us	2
Suspend Latency	Subsector erase	15	30	us	2
Suspend Latency	Erase	15	30	us	3

Notes:

1. Timing is not internally controlled.
2. Any READ command accepted.
3. Any command except the following are accepted: SECTOR, SUBSECTOR, or CHIP ERASE; WRITE STATUS REGISTER; WRITE NONVOLATILE CONFIGURATION REGISTER; and PROGRAM OTP.

10. PACKAGE TYPE INFORMATION

10.1 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 5X5 BALL ARRAY (H)



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

NOTE :

1. Controlling dimension : mm
2. Reference document : JEDEC MO-207

	TITLE	24B 6x8x1.2mm(ball array : 5x5) TF-BGA Package Outline	REV.	B	DATE	03/27/2017

11. ORDERING INFORMATION – Valid Part Numbers

IS25WX 064 _ _ - J H L E :P - TR

PACKING
TR = Tape and Reel
TY = Tray
Blank = Bulk

PBO (Polybenzoxazole) LAYER
:P = Die Overcoat process-PBO layer (Call Factory)

TEMPERATURE RANGE
E = Extended (-40°C to +105°C)
A3 = Automotive Grade (-40°C to +125°C)

PACKAGING CONTENT
L = Green Package (RoHS Compliant, Halogen-free) and TSCA Compliant

PACKAGE Type
H = 24-ball TFBGA (6x8mm) 5x5 ball array
W = KGD (Call Factory)

Option
J = Standard (Default Extended SPI mode)
O = Default Octal DDR mode
W= Dedicated W# (Call Factory)
U= Optional PSC feature (Call Factory)
L= Optional Read while Program/Erase (Call Factory)

Die Revision
Blank = First Gen.

Density
064 = 64 Megabit
032 = 32 Megabit (Call Factory)

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
25LX = FLASH, 2.70V ~ 3.60V, OPI & On-Chip ECC
25WX = FLASH, 1.70V ~ 2.0V, OPI & On-Chip ECC

Note:
1. **Call Factory for other package options available**

Density, Voltage	Frequency (MHz)	Order Part Number	Package
64Mb, 1.8V	166MHz (3)	IS25WX064-JHLE	24-ball TFBGA 6x8mm 5x5 ball array
		IS25WX064-OHLE	24-ball TFBGA 6x8mm 5x5 ball array
		IS25WX064-JHLA3	24-ball TFBGA 6x8mm 5x5 ball array
		IS25WX064-OHLA3	24-ball TFBGA 6x8mm 5x5 ball array

Density, Voltage	Frequency (MHz)	Order Part Number	Package
64Mb, 3.0V	133MHz	IS25LX064-JHLE	24-ball TFBGA 6x8mm 5x5 ball array
		IS25LX064-OHLE	24-ball TFBGA 6x8mm 5x5 ball array
		IS25LX064-JHLA3	24-ball TFBGA 6x8mm 5x5 ball array
		IS25LX064-OHLA3	24-ball TFBGA 6x8mm 5x5 ball array

Notes:
1. A3 meets AEC-Q100 requirements with PPAP.
2. Temp Grades: E= -40 to 105°C, A3= -40 to 125°C.
3. Call Factory for 200MHz