DATA SHEET

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OM7560A

12-bit, 40 Msps analog-to-digital interface for CCD cameras for High Reliability Applications

Data sheet 2013 Feb 25

IDT
Integrated Device Technology

12-bit, 40 Msps analog-to-digital interface for CCD cameras

OM7560A

FEATURES

- Clamp and Track/Hold (CTH) circuit with adjustable bandwidth, Programmable Gain Amplifier (PGA), 12-bit Analog-to-Digital Converter (ADC) and reference regulator
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 40 MHz
- PGA gain from 0 to 36 dB (in 0.05 dB steps)
- CTH programmable bandwidth from 35 to 284 MHz typical
- Standby mode (20 mW typical)
- Low power consumption of only 425 mW typical
- 5 V operation and 2.5 to 5.25 V operation for the digital outputs
- TTL compatible inputs; TTL and CMOS compatible outputs.

APPLICATIONS

- CCD camera systems.

GENERAL DESCRIPTION

The OM7560A is a 12-bit analog-to-digital interface for a CCD camera. The device includes a CTH circuit, PGA and a low-power 12-bit ADC, together with its reference voltage regulator.

The CTH has a bandwidth circuit controlled by on-chip DACs via a serial interface.

A 10-bit digital clamp controls the ADC input clamp level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM7560AHC	CQFP48	ceramic quad flat package; 48 leads; body 8 × 8 × 1 mm	-

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5	5.25	V
V_{CCD}	digital supply voltage		4.75	5	5.25	V
V_{CCO}	digital output supply voltage		2.5	3	5.25	V
I_{CCA}	analog supply current	with internal regulator	–	65	–	mA
I_{CCD}	digital supply current	with internal regulator	–	19	–	mA
I_{CCO}	digital output supply current	f_{pix} = 40 MHz; C_L = 10 pF on all data outputs; ramp input	–	1	–	mA
ADC_{res}	ADC resolution		–	12	–	bits
$V_{i(IN)(p-p)}$	CTH input voltage (peak-to-peak value)		–	2	–	V
G_{CTH}	CTH output amplifier gain		–	0	–	dB
PGA_{dyn}	PGA dynamic range		–	36	–	dB
$f_{pix(max)}$	maximum pixel frequency	code $f_{co(CTH)}$ = 0000	40	–	–	MHz
$N_{tot(rms)}$	total noise from CTH input to ADC output (RMS value)	G_{PGA} = 0 dB; code $f_{co(CTH)}$ = 0000	–	0.85	–	LSB
$V_{n(i)(eq)(rms)}$	equivalent input noise (RMS value)	G_{PGA} = 30 dB; code $f_{co(CTH)}$ = 0000; note 1	–	90	–	μV
P_{tot}	total power consumption		–	425	–	mW

Note

1. Noise and clamp behaviour are not guaranteed for a PGA gain higher than 30 dB.

BLOCK DIAGRAM

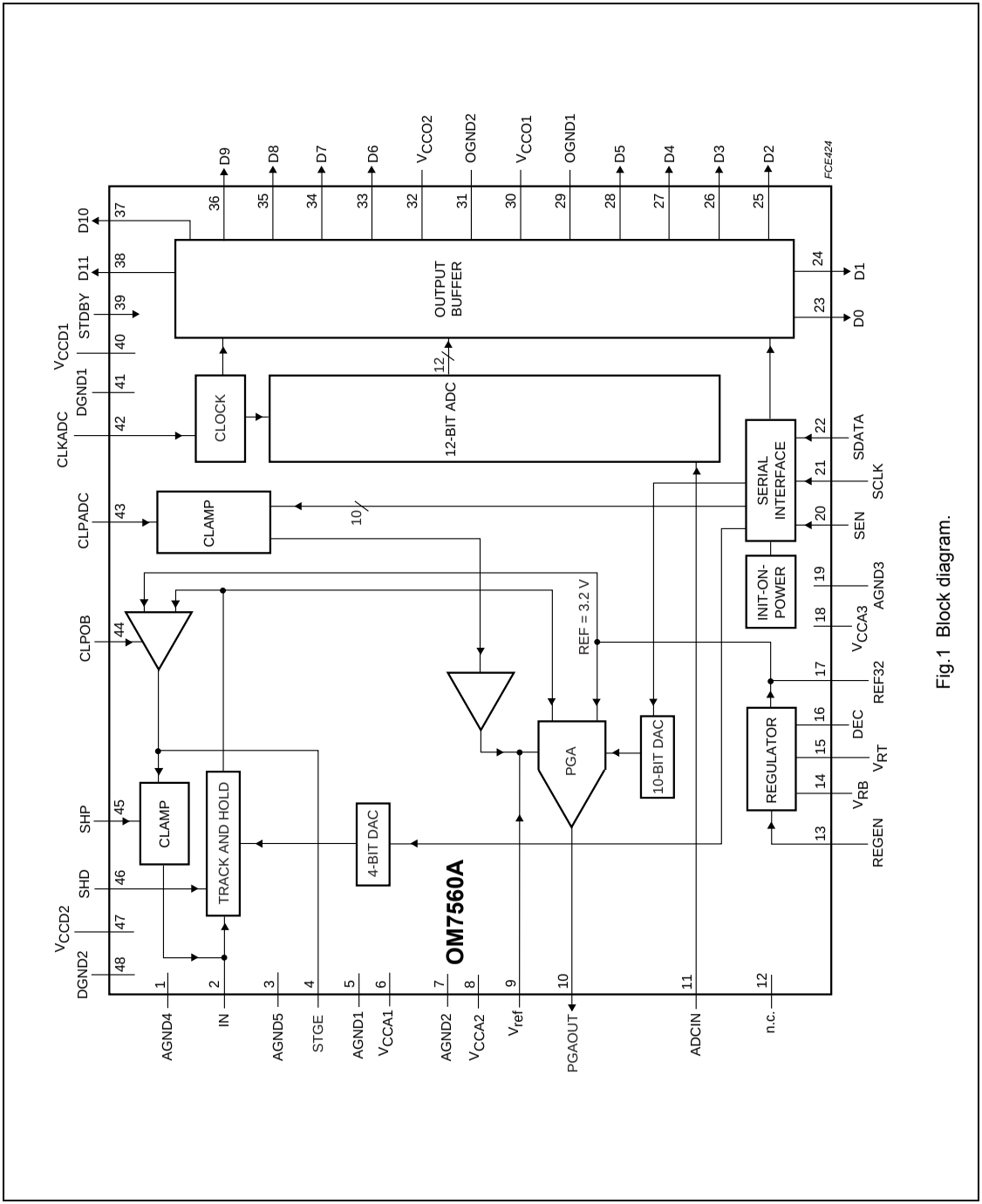


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGND4	1	analog ground 4
IN	2	data input signal from CCD
AGND5	3	analog ground 5
STGE	4	clamp storage capacitor pin
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
AGND2	7	analog ground 2
V_{CCA2}	8	analog supply voltage 2
V_{ref}	9	ADC clamp reference voltage input; short-circuited to ground via a capacitor
PGAOUT	10	PGA amplifier signal output
ADCIN	11	ADC analog signal input; externally connected to pin PGAOUT
n.c.	12	not connected
REGEN	13	regulator enable input (active HIGH)
V_{RB}	14	regulator reference voltage bottom
V_{RT}	15	regulator reference voltage top
DEC	16	regulator decoupling; decoupled to ground via a capacitor
REF32	17	internal reference voltage; decoupled to ground via a capacitor
V_{CCA3}	18	analog supply voltage 3
AGND3	19	analog ground 3
SEN	20	enable input for the serial interface shift register (active LOW)
SCLK	21	serial clock input for the serial interface
SDATA	22	serial data input: 10-bit PGA gain, 4-bit DAC for the frequency cut-off, 10 low significant bits for the digital ADC clamp and edge pulse control
D0	23	ADC digital output 0 (LSB)
D1	24	ADC digital output 1
D2	25	ADC digital output 2
D3	26	ADC digital output 3
D4	27	ADC digital output 4
D5	28	ADC digital output 5
OGND1	29	digital output ground 1
V_{CCO1}	30	digital output supply voltage 1
OGND2	31	digital output ground 2
V_{CCO2}	32	digital output supply voltage 2
D6	33	ADC digital output 6
D7	34	ADC digital output 7
D8	35	ADC digital output 8
D9	36	ADC digital output 9
D10	37	ADC digital output 10
D11	38	ADC digital output 11 (MSB)
STDBY	39	standby control input (active HIGH); all output bits are logic 0 when standby is enabled

SYMBOL	PIN	DESCRIPTION
V_{CCD1}	40	digital supply voltage 1
DGND1	41	digital ground 1
CLKADC	42	ADC clock input
CLPADC	43	clamp control pulse input for ADC analog input signal
CLPOB	44	clamp control pulse input at optical black
SHP	45	preset sample and hold pulse input
SHD	46	data sample and hold pulse input
V_{CCD2}	47	digital supply voltage 2
DGND2	48	digital ground 2

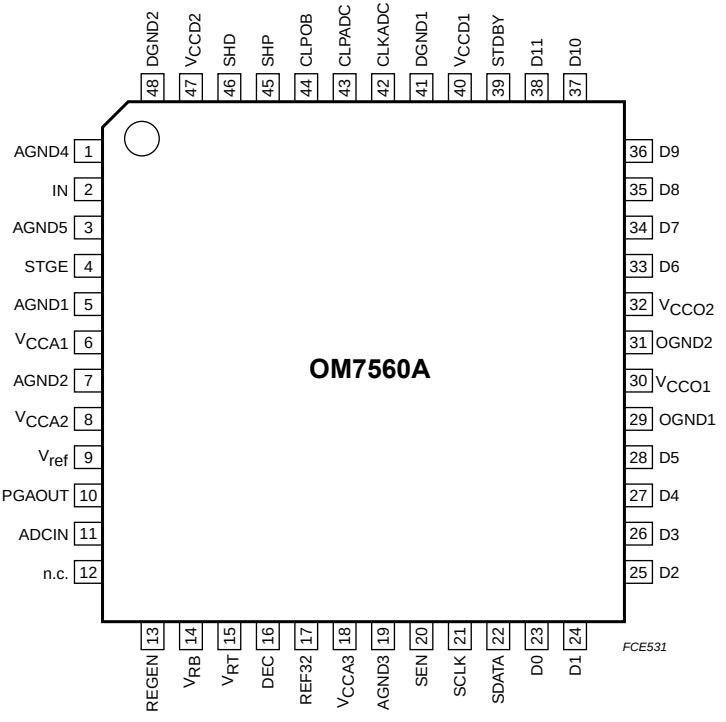


Fig.2 Top View Pin Configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	digital output supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	between V_{CCA} and V_{CCD}		−1.0	+1.0	V
	between V_{CCD} and V_{CCO}		−1.0	+4.0	V
V_i	input voltage	referenced to AGND	−0.3	+7.0	V
I_o	output current		−10	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−50	+110	°C
T_j	junction temperature		−	150	°C

Note

1. All supplies are connected together.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	structure without adhesive between package andf PCB	**14.4**	°C/W

CHARACTERISTICS

V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3 V; f_{pix} = 40 MHz; T_{amb} = −50 to +110 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5	5.25	V
V_{CCD}	digital supply voltage		4.75	5	5.25	V
V_{CCO}	digital output supply voltage		2.5	3	5.25	V
I_{CCA}	analog supply current	with internal regulator	–	65	–	mA
I_{CCD}	digital supply current	with internal regulator	–	19	–	mA
I_{CCO}	digital output supply current	f_{pix} = 40 MHz; C_L = 10 pF on all data outputs; ramp input	–	1	–	mA
Digital inputs						
CLOCK INPUT: PIN CLKADC (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLKADC} = 0.8 V	−1	–	+1	μA
I_{IH}	HIGH-level input current	V_{CLKADC} = 2.0 V	–	–	20	μA
Z_i	input impedance		–	63	–	kΩ
C_i	input capacitance		–	1	–	pF
CONTROL INPUTS: PINS SEN, SCLK, SDATA, STDBY, CLPOB, CLPADC AND REGEN						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_i	input current		−2	–	+2	μA
SAMPLE AND HOLD INPUTS: PINS SHP AND SHD						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_i	input current		−10	–	+10	μA
Clamp and Track/Hold (CTH) circuit: pins IN, SHD and SHP						
$V_{i(IN)(p-p)}$	CTH input voltage (peak-to-peak value)		–	2	–	V
$I_{i(IN)}$	input current		−3	–	+3	μA
$t_{W(SHP)}$	SHP pulse width	$V_{i(IN)}$ = 1000 mV; transition (98.5%) in 1 pixel; code $f_{co(CTH)}$ = 0000; see Fig.5	–	7	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{W(SHD)}$	SHD pulse width	$V_{i(IN)}$ = 1000 mV; transition (98.5%) in 1 pixel; code $f_{co(CTH)}$ = 0000; see Fig.5	–	8	–	ns
		code $f_{co(CTH)}$				
		0001	–	12	–	ns
		0010	–	16	–	ns
		0100	–	22	–	ns
		1000	–	32	–	ns
		1111	–	49	–	ns
$t_{h(IN-SHP)}$	CTH input hold time compared to control pulse SHP	see Fig.5	–	3	–	ns
$t_{h(IN-SHD)}$	CTH input hold time compared to control pulse SHD	see Fig.5	–	3	–	ns
Programmable Gain Amplifier (PGA) output: pin PGAOUT						
$V_{PGAOUT(p-p)}$	PGA output amplifier dynamic voltage level (peak-to-peak value)		–	2000	–	mV
$V_{PGAOUT(b)}$	PGA output amplifier black level voltage	code $C_{(CLP)}$ = 0	–	1.475	–	V
Z_{PGAOUT}	PGA output amplifier output impedance	f_{pix} at 10 kHz for minimum and maximum values	–	5	–	Ω
I_{PGAOUT}	PGA output current drive	static	–	–	1	mA
$G_{PGA(min)}$	minimum gain of PGA circuit	code G_{PGA} = 0	–	0	–	dB
$G_{PGA(max)}$	maximum gain of PGA circuit	code G_{PGA} ≥767	–	36	–	dB
Analog-to-Digital Converter (ADC)						
$f_{pix(max)}$	maximum pixel frequency			–	–	MHz
$t_{W(CLKADC)H}$	CLKADC pulse width HIGH	$V_{i(IN)}$ = 1000 mV; transition (99.5%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 128; see Fig.5	–	11	–	ns
$t_{W(CLKADC)L}$	CLKADC pulse width LOW	$V_{i(IN)}$ = 1000 mV; transition (99.5%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 128	–	11	–	ns
SR_{CLKADC}	CLKADC input slew rate	rising and falling edges; 10% to 90%	0.5	–	–	V/ns
$V_{i(ADCIN)(p-p)}$	ADC input voltage (peak-to-peak value)	with internal regulator	–	2	–	V
$I_{i(ADCIN)}$	ADC input current		–2	–	+120	μA
V_{RB}	ADC reference voltage bottom		–	1.30	–	V
V_{RT}	ADC reference voltage top		–	3.65	–	V
DNL	differential non linearity	ramp input; f_{pix} = 40 MHz; no missing code	–	–	+2.0 -0.9	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d(s)}$	sampling delay	see Fig.5	–	–	6	ns
Total chain characteristics (CTH + PGA + ADC)						
$t_{d(SHD-CLKADC)}$	delay between SHD and CLKADC	$V_{i(IN)}$ = 1000 mV; transition (95%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 128; see Fig.5	–	15	–	ns
$t_{h(SHD-CLKADC)}$	SHD hold time compared to CLKADC	$V_{i(IN)}$ = 32 mV; transition (95%) in 1 pixel; code $f_{co(CTH)}$ = 0000; code G_{PGA} = 767; see Fig.5	–	0	–	ns
$N_{tot(rms)}$	total noise from CTH input to ADC output (RMS value)	G_{PGA} = 0 dB; code $f_{co(CTH)}$ = 0000	–	0.85	–	LSB
		G_{PGA} = 30 dB; code $f_{co(CTH)}$ = 0000; note 1	–	6	–	LSB
$O_{CCD(max)}$	maximum offset voltage between CCD floating level and CCD dark pixel level	see Fig.11	−200	–	+200	mV
$V_{n(i)(eq)(rms)}$	equivalent input noise (RMS value)	G_{PGA} = 30 dB; code $f_{co(CTH)}$ = 0000; note 1	–	90	–	μV
Digital outputs (f_{pix} = 40 MHz; C_L = 10 pF)						
V_{OH}	HIGH-level output voltage	I_{OH} = −1 mA	V_{CCO} − 0.5	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
$t_{h(o)}$	output hold time	see Fig.5	10	–	–	ns
$t_{d(o)}$	output delay	V_{CCO} = 5.25 V	–	20	–	ns
		V_{CCO} = 3 V	–	26	–	ns
Serial interface						
$f_{SCLK(max)}$	maximum clock frequency of serial interface		5	–	–	MHz

Note

1. Noise and clamp behaviour are not guaranteed for a PGA gain higher than 30 dB.

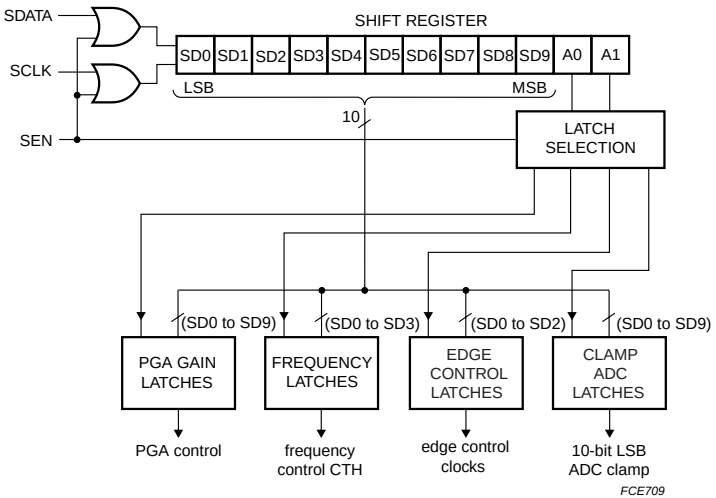
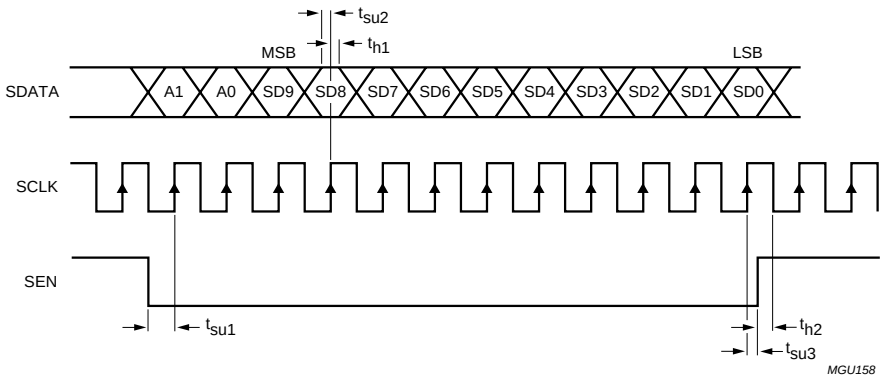


Fig.3 Serial interface block diagram.



$t_{su1} = t_{su2} = t_{su3} = 4$ ns (minimum);
$t_{h1} = t_{h2} = 4$ ns (minimum).

Fig.4 Loading sequence of control DACs input data via the serial interface.

Table 1 Serial interface programming

ADDRESS BITS		SDATA BITS SD0 to SD9
A1	**A0**	
0	0	clamp reference of ADC (SD0 to SD9), note 1
0	1	cut-off frequency of CTH (SD0 to SD3)
1	0	PGA gain control (SD0 to SD9)
1	1	edge control for pulses SHP, SHD, CLPOB, CLPADC and CLKADC (note 2): SD0 = 1, SHP and SHD sample on LOW level SD1 = 1, CLPADC and CLPOB activated on HIGH level SD2 = 1, CLKADC activated with rising edge

Notes

1. PGA gain register must always be refreshed after clamp code register content has been changed.
2. When pin CLPADC = HIGH (SD1 = 1; serial interface), the ADC input is clamped to the voltage level of V_{ref}. Pin V_{ref} is connected to ground via a capacitor.

When the power supplies increase from zero to V_{CC}, the init-on-power block initializes the circuit as follows:

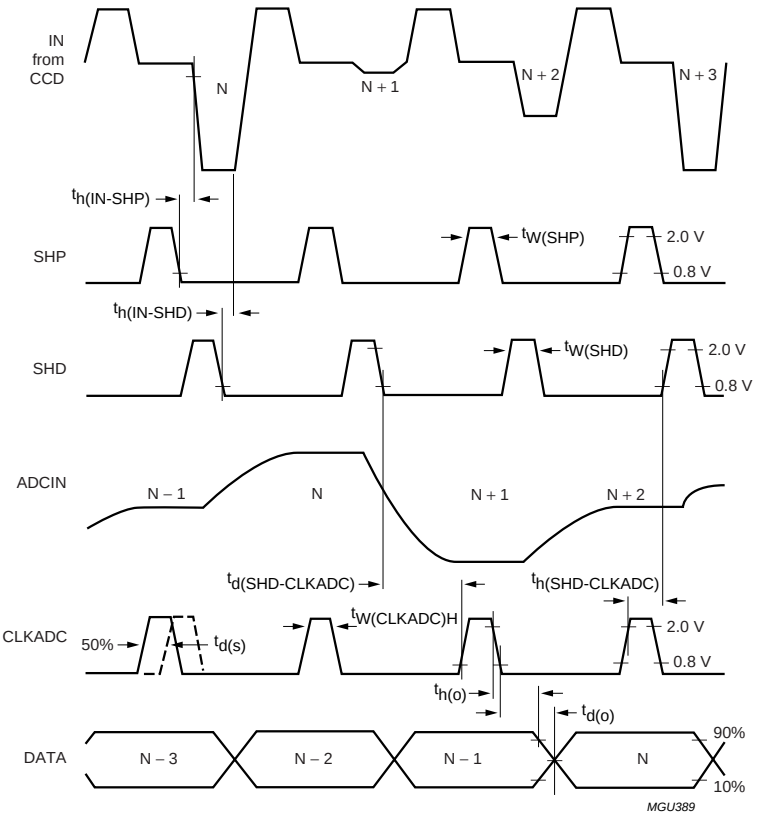
- Cut-off frequency of the CTH circuit is set to: code $f_{co(CTH)} = 0$
- PGA gain control is set to: code $G_{PGA} = 0$
- Clamp code of the ADC is set to: code $ADC_{CLP} = 0$
- SHP and SHD sample on HIGH level; CLKADC activated with rising edge
- CLPOB and CLPADC activated on HIGH level.

Table 2 Standby selection

PIN STDBY	DATA BITS SD9 to SD0	$I_{CCA} + I_{CCD}$
HIGH	logic 0	4 mA (typical); note 1
LOW	active	84 mA (typical)

Note

1. In case an external regulator is used, it has to be switched off in standby mode in order to avoid an extra power consumption of the OM7560A.



The polarities used in this case are:
- SHP and SHD sample on HIGH level
- CLKADC activated with rising edge.

Fig.5 Pixel frequency timing diagram.

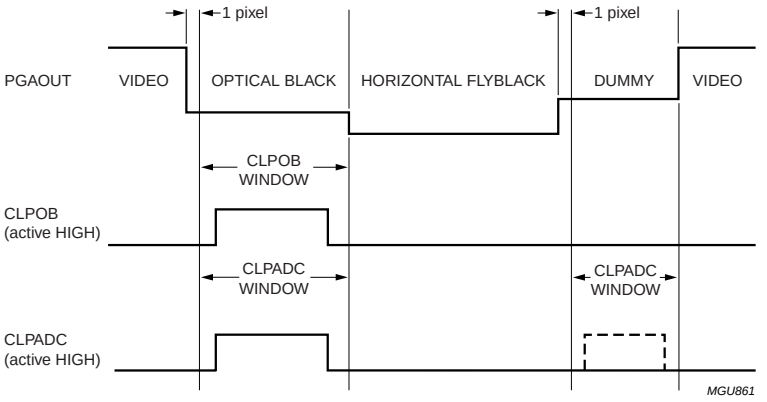


Fig.6 Line frequency timing diagram.

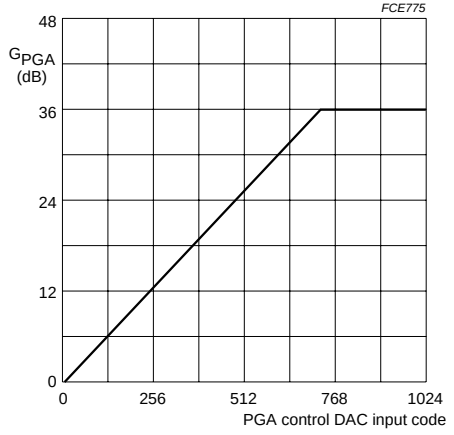


Fig.7 PGA gain as a function of PGA control DAC input code.

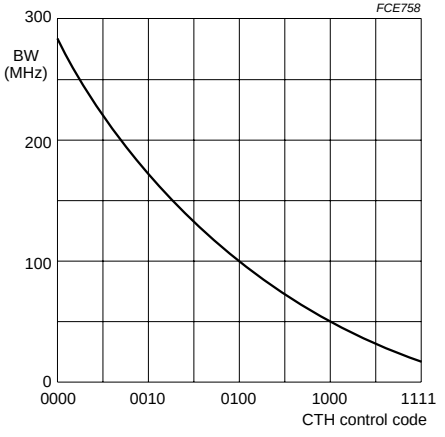


Fig.8 CTH bandwidth as a function of CTH control code.

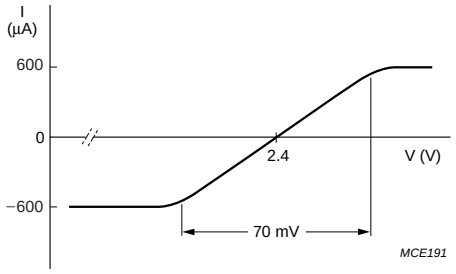
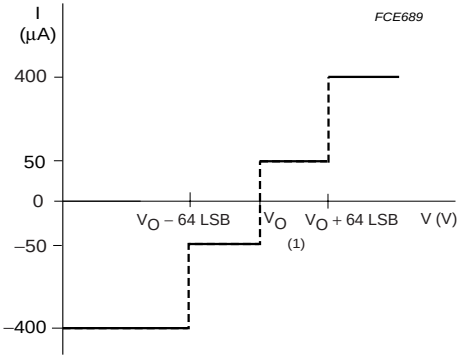


Fig.9 Typical clamp current as a function of voltage on pin STGE.



(1) V_O depends on the clamp code.

Fig.10 Typical clamp current as a function of voltage on pin V_{ref}.

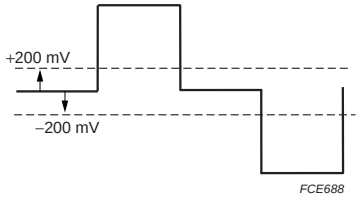
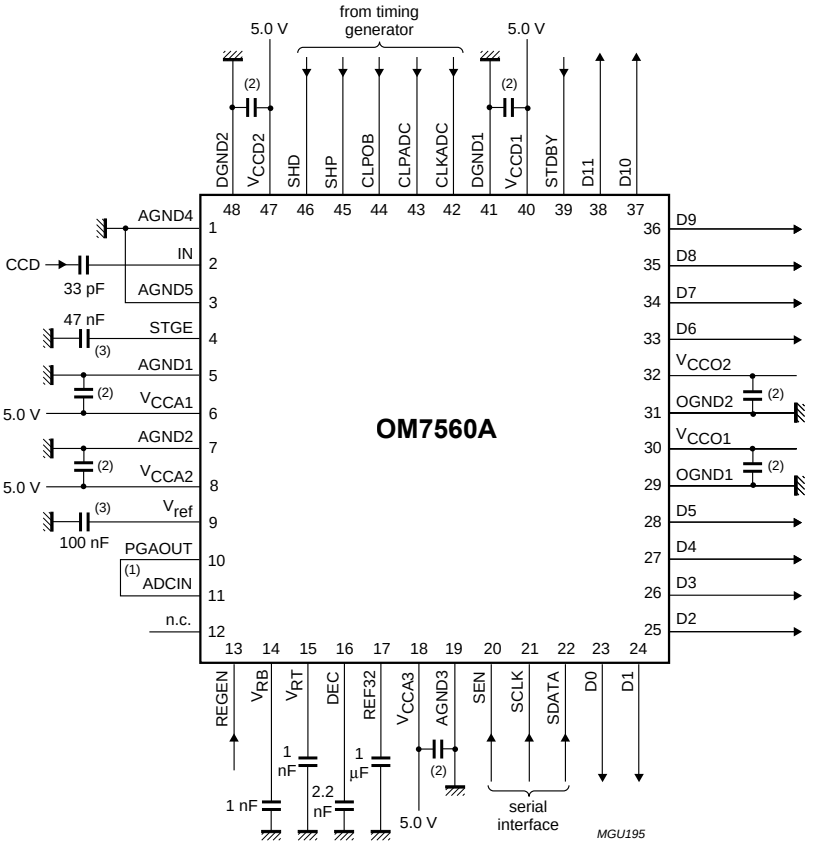


Fig.11 Maximum offset voltage between CCD floating and dark pixel level.

APPLICATION DIAGRAM



(1) The clamp level of the signal input at pin ADCIN can be tuned from code 0 to code 1023 in one LSB step of the ADC via the serial interface (clamp ADC activated).

(2) All supply pins must be decoupled with 100 nF capacitors as closely as possible to the device.

(3) The capacitors on pins STGE and V_{ref} have typical values, performing a typical device start-up time of 300 µs from standby to active (supplies on).

Fig.12 Application diagram.

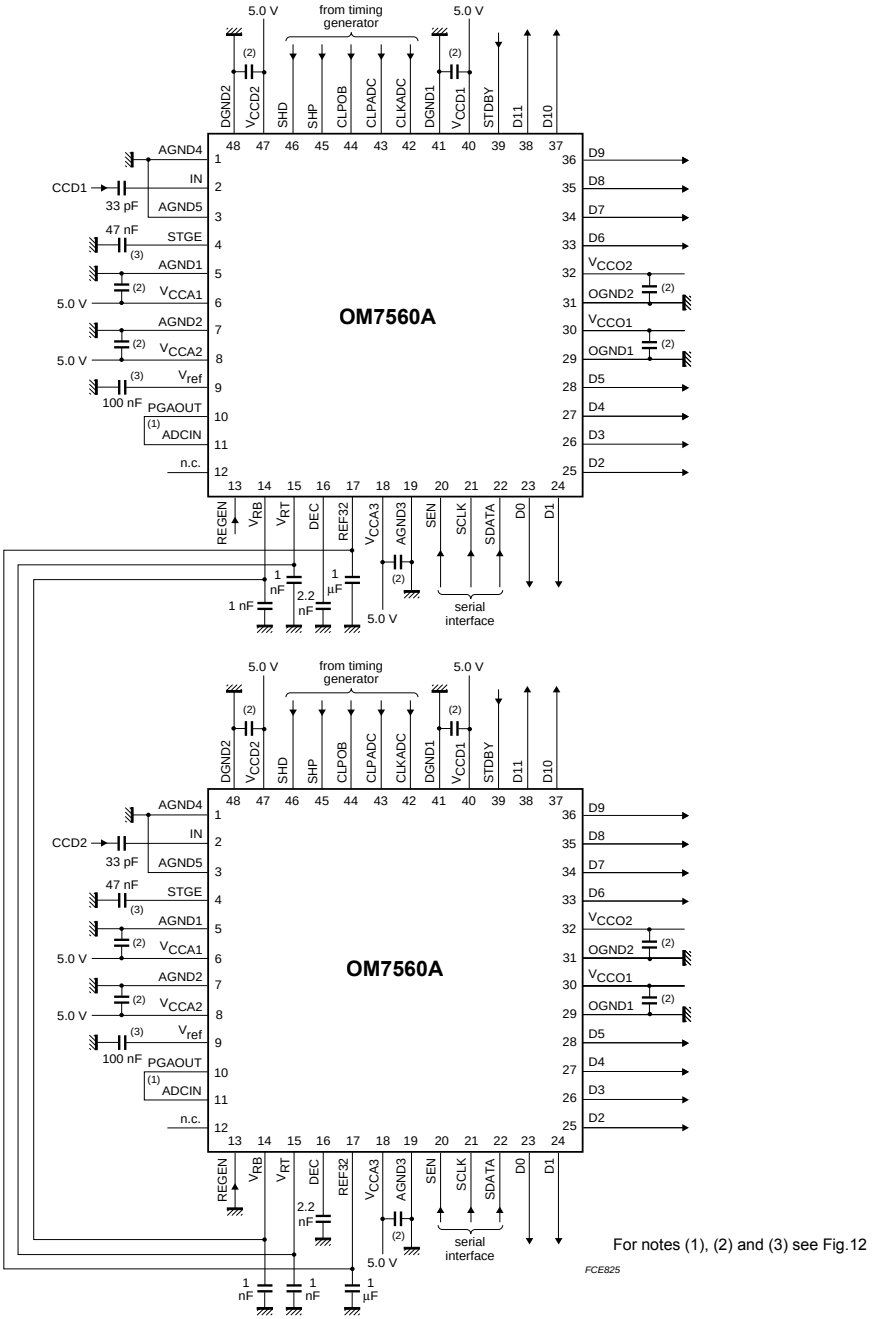


Fig.13 Application diagram with 2 CCDs.

Power and grounding recommendations

Care must be taken to minimize noise when designing a printed-circuit board for applications such as PC cameras, surveillance cameras, camcorders and digital still cameras.

For the front-end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as classical operational amplifiers) must be taken into account, particularly with respect to power and ground connections.

The connections between CCD interface and CTH input should be as short as possible and a ground ring protection around these connections can be beneficial.

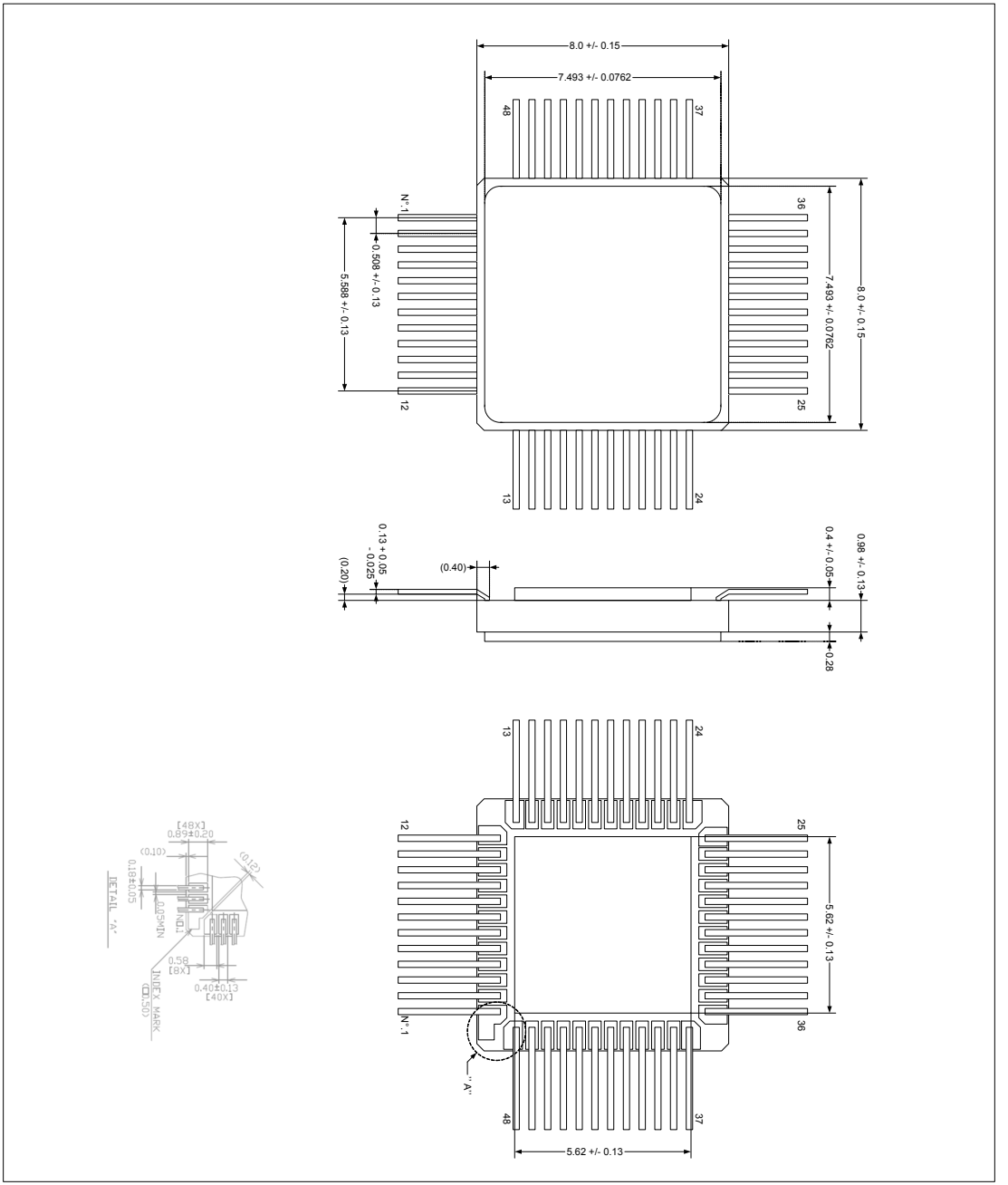
Separate analog and digital supplies provide the best performance. If it is not possible to do this on the board, then decouple the analog supply pins effectively from the digital supply pins. The decoupling capacitors must be placed as close as possible to the IC package.

In a two-ground system, in order to minimize the noise from package and die parasitics, the following recommendations must be implemented:

- The ground pin associated with the digital outputs must be connected to the digital ground plane and special care should be taken to avoid feedthrough in the analog ground plane. The analog and digital ground planes must be connected with an inductor as close as possible to the IC package, in order to have the same DC voltage on the ground planes.
- The digital output pins and their associated lines should be shielded by the digital ground plane, which can be used as return path for the digital signals.

PACKAGE OUTLINE

CQFP48: ceramic quad flat package; 48 leads



MARKING

Top view
M7560: Part number
WW-YY: date code (week + year)
●: Pin1 indicator

Bottom view
ZZZZ: Serial number

Pin1 indicator

HIGH RELIABILITY PRODUCT CAPABILITY

OM7560A is a commercial-of-the-shelf (COTS) solution for High Reliability application with the following additional key features:

- Extended operating temperature range,
- Hermetic packaging with unique serialization tag,
- Manufacturing traceability (wafer processing, assembly),
- 100% burn-in,
- Lot validation testing.

OM7560A is processed according to the methods of the latest revision of ESCC Generic Specification 9000.

EXCEPTIONS TO ESCC GENERIC SPECIFICATION 9000 SECIFICATION

OM7560A is not fully compliant to ESCC Generic Specification 9000 since IDT has not evaluated OM7560A Dose Radiation Testing product capability.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integrated Device Technology customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integrated Device Technology for any damages resulting from such application.

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