# G3R45MT17-CAL
# 1700 V 45 mΩ SiC MOSFET

**GeneSiC™**
SEMICONDUCTOR

## Silicon Carbide MOSFET
### N-Channel Enhancement Mode

For physical chip dimensions please contact engineering@diedevices.com

| | | |
|---|---|---|
| $V_{DS}$ | = | 1700 V |
| $R_{DS(ON)(Typ.)}$ | = | 45 mΩ |
| $I_{D(T_C = 100°C)}$ | = | 40 A |

## Features

- G3R™ Technology with +15 V Gate Drive
- Softer $R_{DS(ON)}$ v/s Temperature Dependency
- LoRing™ - Electromagnetically Optimized Design
- Smaller $R_{G(INT)}$ and Lower $Q_G$
- Low Device Capacitances ($C_{OSS}$, $C_{RSS}$)
- Superior Cost-Performance Index
- Robust Body Diode with Low $V_F$ and Low $Q_{RR}$
- Industry-Leading UIL & Short-Circuit Robustness

## Bare Chip
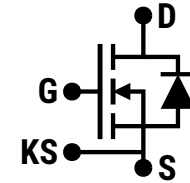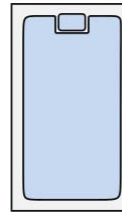
D = Drain
G = Gate
S = Source
KS = Kelvin Source

RoHS

REACH

## Advantages

- Compatible with Commercial Gate Drivers
- Low Conduction Losses at all Temperatures
- Reduced Ringing
- Faster and More Efficient Switching
- Lesser Switching Spikes and Lower Losses
- Better Power Density and System Efficiency
- Ease of Paralleling without Thermal Runaway
- Higher System Reliability

## Applications

- Electric Vehicle Fast Charging
- Solar Inverters
- Traction Inverters
- Smart Grid and HVDC
- High Voltage DC-DC Converters
- Switched Mode Power Supply
- Wind Energy Converters
- Pulsed Power

## Absolute Maximum Ratings (At $T_C$ = 25°C Unless Otherwise Stated)

| Parameter | Symbol | Conditions | Values | Unit | Note |
|---|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS(max)}$ | $V_{GS}$ = 0 V, $I_D$ = 100 µA | 1700 | V | |
| Gate-Source Voltage (Dynamic) | $V_{GS(max)}$ | | -10 / +20 | V | |
| Gate-Source Voltage (Static) | $V_{GS(op)}$ | Recommended Operation | -5 / +15 | V | |
| Continuous Forward Current | $I_D$ | $T_C$ = 25°C, $V_{GS}$ = -5 / +15 V | 53 | A | |
| | | $T_C$ = 100°C, $V_{GS}$ = -5 / +15 V | 40 | | |
| | | $T_C$ = 135°C, $V_{GS}$ = -5 / +15 V | 32 | | |
| Pulsed Drain Current | $I_{D(pulse)}$ | $t_P$ ≤ 3µs, D ≤ 1%, $V_{GS}$ = 15 V, Note 1 | 120 | A | |
| Power Dissipation | $P_D$ | $T_C$ = 25°C | 425 | W | Note 2 |
| Non-Repetitive Avalanche Energy | $E_{AS}$ | L = 3.9 mH, $I_{AS}$ = 17.5 A | 592 | mJ | |
| Operating and Storage Temperature | $T_j$ , $T_{stg}$ | | -55 to 200 | °C | |

*Note 1: Pulse Width $t_P$ Limited by $T_{j(max)}$*

## Electrical Characteristics (At $T_C$ = 25°C Unless Otherwise Stated)

| Parameter | Symbol | Conditions | Values | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Drain-Source Breakdown Voltage | $V_{DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 100 µA | 1700 | | | V | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 1700 V, $V_{GS}$ = 0 V | | 1 | | µA | |
| Gate Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | 100 | nA | |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = -10 V | | | -100 | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 30.0 mA | 1.8 | 2.70 | | V | Fig. 9 |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = 30.0 mA, $T_j$ = 200°C | | 1.85 | | | |
| Transconductance | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 35 A | | 16.8 | | S | Fig. 4 |
| | | $V_{DS}$ = 10 V, $I_D$ = 35 A, $T_j$ = 200°C | | 16.6 | | | |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$ = 15 V, $I_D$ = 35 A | | 45 | 62 | mΩ | Fig. 5-8 |
| | | $V_{GS}$ = 15 V, $I_D$ = 35 A, $T_j$ = 200°C | | 108 | | | |
| Input Capacitance | $C_{iss}$ | | | 3199 | | pF | Fig. 11 |
| Output Capacitance | $C_{oss}$ | | | 86 | | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 15.3 | | | |
| $C_{oss}$ Stored Energy | $E_{oss}$ | $V_{DS}$ = 1000 V, $V_{GS}$ = 0 V | | 57 | | µJ | Fig. 12 |
| $C_{oss}$ Stored Charge | $Q_{oss}$ | f = 1 MHz, $V_{AC}$ = 25mV | | 172 | | nC | |
| Effective Output Capacitance (Energy Related) | $C_{o(er)}$ | | | 114 | | pF | Note 3 |
| Effective Output Capacitance (Time Related) | $C_{o(tr)}$ | | | 172 | | | |
| Gate-Source Charge | $Q_{gs}$ | $V_{DS}$ = 1000 V, $V_{GS}$ = -5 / +15 V | | 33 | | nC | Fig. 10 |
| Gate-Drain Charge | $Q_{gd}$ | $I_D$ = 35 A | | 37 | | | |
| Total Gate Charge | $Q_g$ | Per IEC607478-4 | | 106 | | | |
| Internal Gate Resistance | $R_{G(int)}$ | f = 1 MHz, $V_{AC}$ = 25 mV | | 1.3 | | Ω | |
| Turn-On Switching Energy (Body Diode) | $E_{On}$ | $T_j$ = 25°C; $V_{GS}$ = -5/+15V; $R_{G(ext)}$ = 1 Ω, $I_D$ = 35 A; $V_{DD}$ = 1200 V | | 222 | | µJ | Fig. 18 |
| Turn-Off Switching Energy (Body Diode) | $E_{Off}$ | | | 100 | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 1200 V, $V_{GS}$ = -5/+15V $R_{G(ext)}$ = 1 Ω, $I_D$ = 35 A Timing relative to $V_{DS}$, Resistive load | | 7 | | ns | Fig. 20 |
| Rise Time | $t_r$ | | | 16 | | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 6 | | | |
| Fall Time | $t_f$ | | | 10 | | | |

*The chip technology was characterized up to 200 V/ns. The measured dV/dt was limited by measurement test setup and package.*
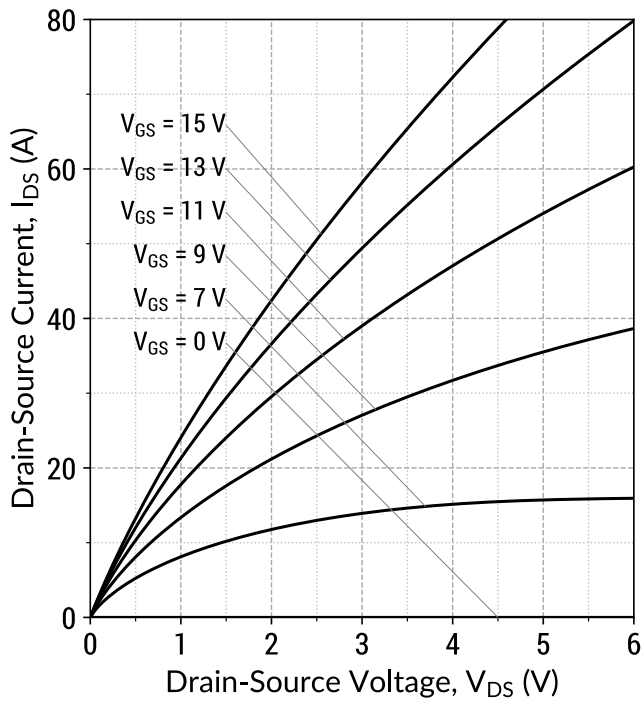
*Note 2: Assuming $Rth_{JC(max)}$ = 0.41°C/W*

*Note 3: $C_{o(er)}$, a lumped capacitance that gives same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 1000V.*

*$C_{o(tr)}$, a lumped capacitance that gives same charging times as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 1000V.*
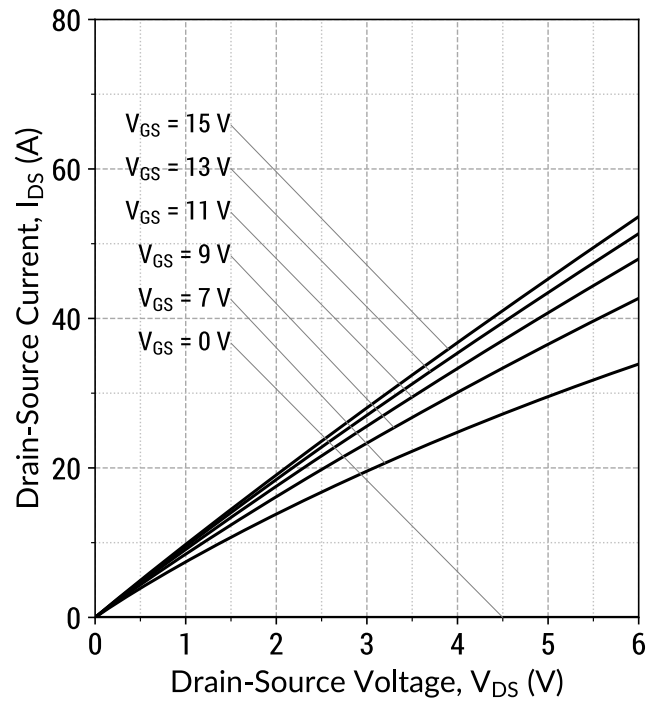
## Reverse Diode Characteristics

| Parameter | Symbol | Conditions | Values | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Diode Forward Voltage | $V_{SD}$ | $V_{GS}$ = -5 V, $I_{SD}$ = 17 A | | 4.5 | | V | Fig. 13-14 |
| | | $V_{GS}$ = -5 V, $I_{SD}$ = 17 A, $T_j$ = 200°C | | 4.3 | | | |
| Continuous Diode Forward Current | $I_S$ | $V_{GS}$ = -5 V, $T_c$ = 100°C | 41 | | | A | |
| Diode Pulse Current | $I_{S(pulse)}$ | $V_{GS}$ = -5 V, Note 1 | | 164 | | A | |
| Reverse Recovery Time | $t_{rr}$ | $V_{GS}$ = -5 V, $I_{SD}$ = 35 A, $V_R$ = 1200 V dif/dt = 2200 A/μs, $T_j$ = 25°C | | 31 | | ns | |
| Reverse Recovery Charge | $Q_{rr}$ | | | 305 | | nC | |
| Peak Reverse Recovery Current | $I_{rrm}$ | | | 8 | | A | |
| Reverse Recovery Time | $t_{rr}$ | $V_{GS}$ = -5 V, $I_{SD}$ = 35 A, $V_R$ = 1200 V dif/dt = 2200 A/μs, $T_j$ = 200°C | | 56 | | ns | |
| Reverse Recovery Charge | $Q_{rr}$ | | | 1174 | | nC | |
| Peak Reverse Recovery Current | $I_{rrm}$ | | | 18 | | A | |

## Figure 1: Output Characteristics ($T_j$ = 25°C)



$V_{GS}$ = 15 V
$V_{GS}$ = 13 V
$V_{GS}$ = 11 V
$V_{GS}$ = 9 V
$V_{GS}$ = 7 V
$V_{GS}$ = 0 V

$I_D$ = f($V_{DS}$, $V_{GS}$); $t_P$ = 250 µs

## Figure 2: Output Characteristics ($T_j$ = 200°C)



$V_{GS}$ = 15 V
$V_{GS}$ = 13 V
$V_{GS}$ = 11 V
$V_{GS}$ = 9 V
$V_{GS}$ = 7 V
$V_{GS}$ = 0 V

$I_D$ = f($V_{DS}$, $V_{GS}$); $t_P$ = 250 µs

## Figure 3: Output Characteristics ($V_{GS}$ = 15 V)



$T_j$ = 200°C
$T_j$ = 175°C
$T_j$ = 150°C
$T_j$ = 125°C
$T_j$ = 75°C
$T_j$ = 25°C
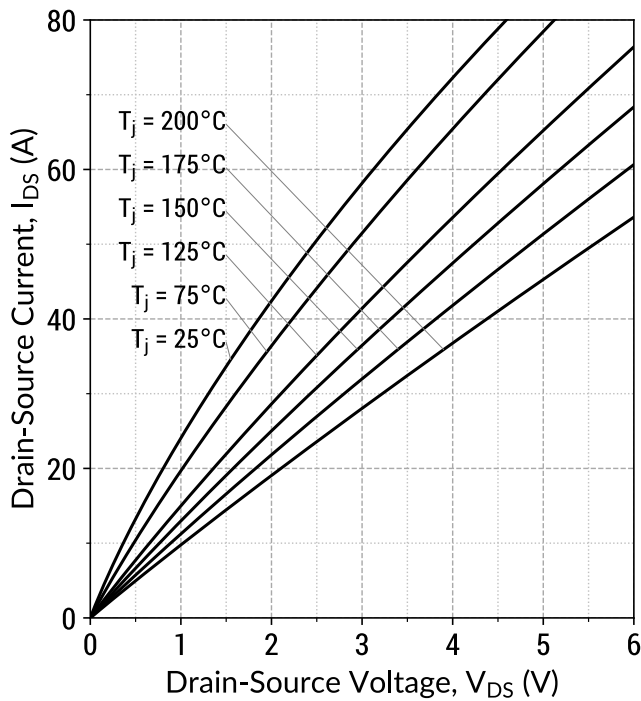
$I_D$ = f($V_{DS}$, $T_j$); $t_P$ = 250 µs

## Figure 4: Transfer Characteristics ($V_{DS}$ = 10 V)



$T_j$ = 200°C
$T_j$ = 25°C
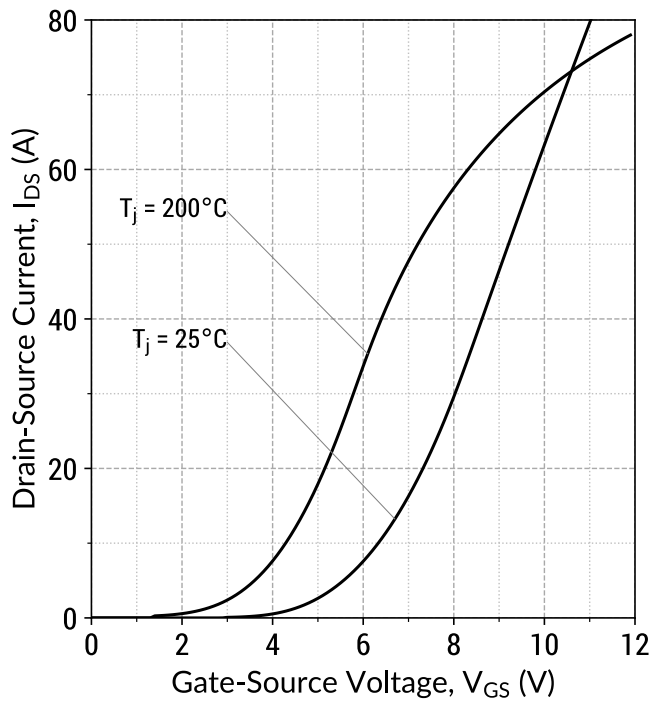
$I_D$ = f($V_{GS}$, $T_j$); $t_P$ = 100 µs

## Figure 5: On-State Resistance v/s Temperature
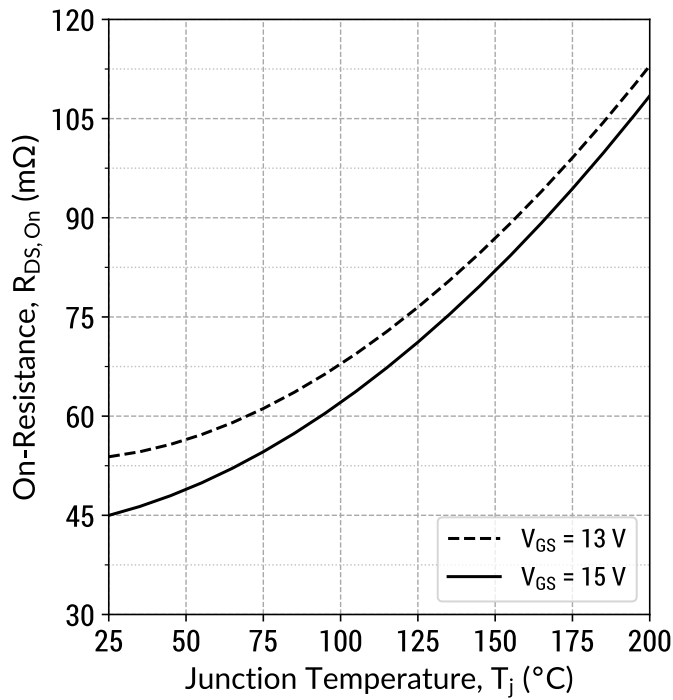


$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 250 \mu s; I_D = 35 A$

## Figure 6: On-State Resistance v/s Drain Current
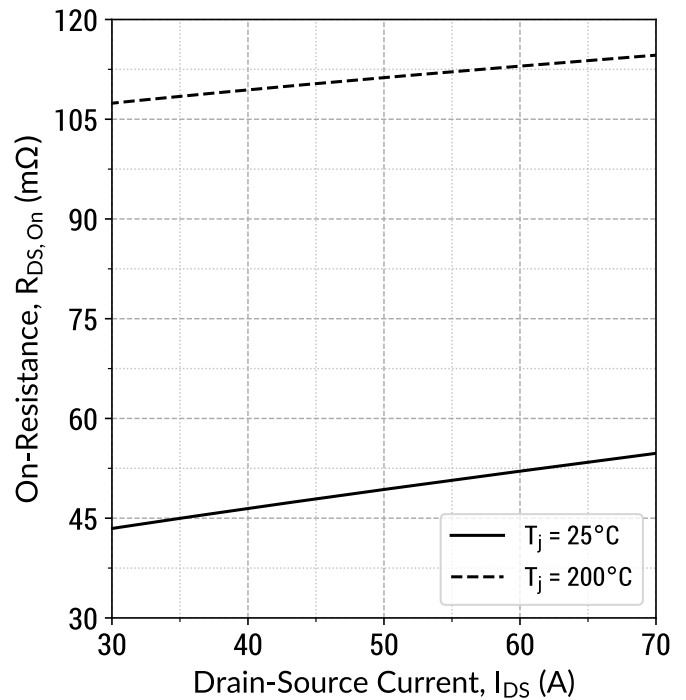


$R_{DS(ON)} = f(T_j, I_D); t_P = 250 \mu s; V_{GS} = 15 V$

## Figure 7: Normalized On-State Resistance v/s Temperature
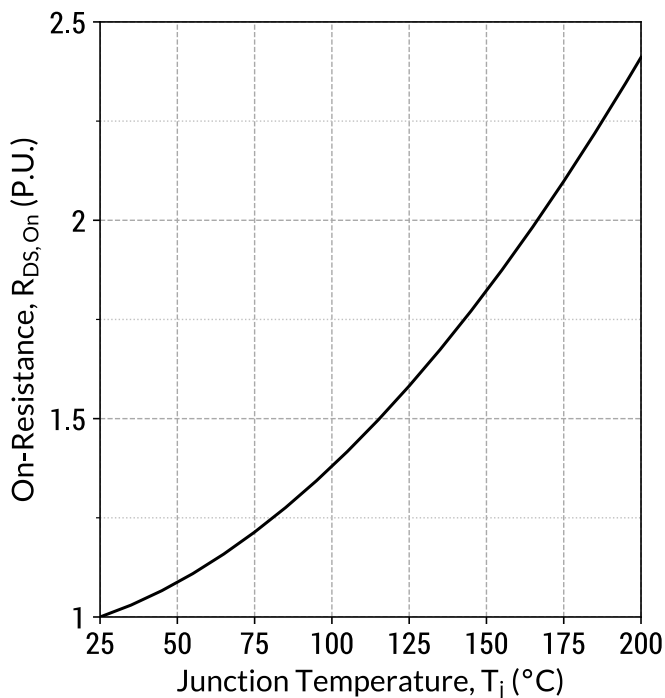


$R_{DS(ON)} = f(T_j); t_P = 250 \mu s; I_D = 35 A; V_{GS} = 15 V$

## Figure 8: On-State Resistance v/s Gate Voltage
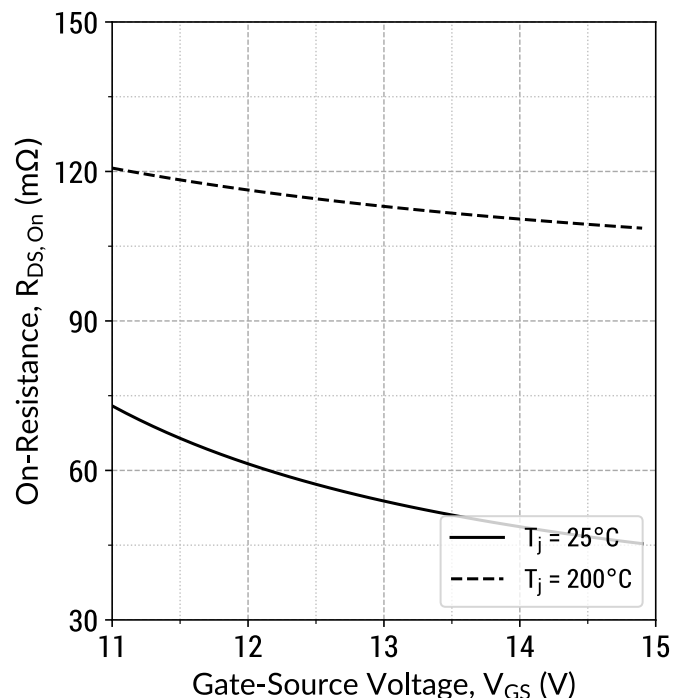


$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 250 \mu s; I_D = 35 A$

## Figure 9: Threshold Voltage Characteristics
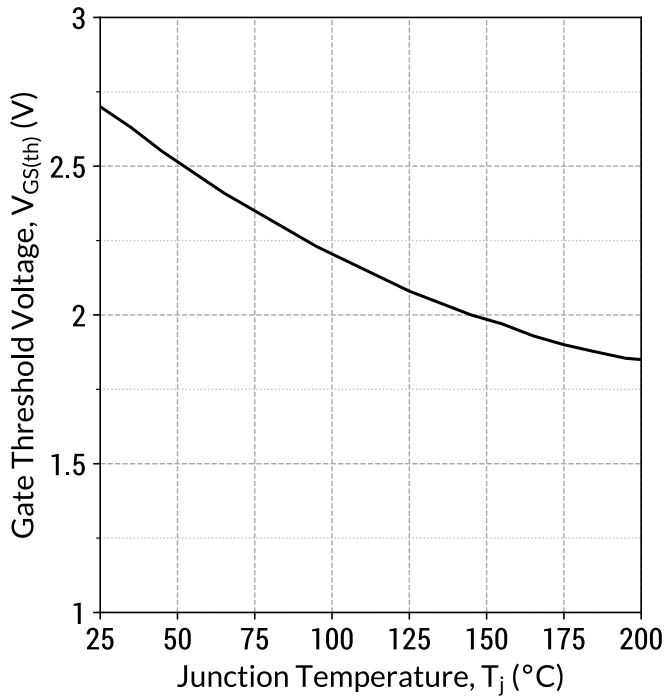


$V_{GS(th)}$ = f($T_j$); $V_{DS}$ = $V_{GS}$; $I_D$ = 30.0 mA

## Figure 10: Gate Charge Characteristics
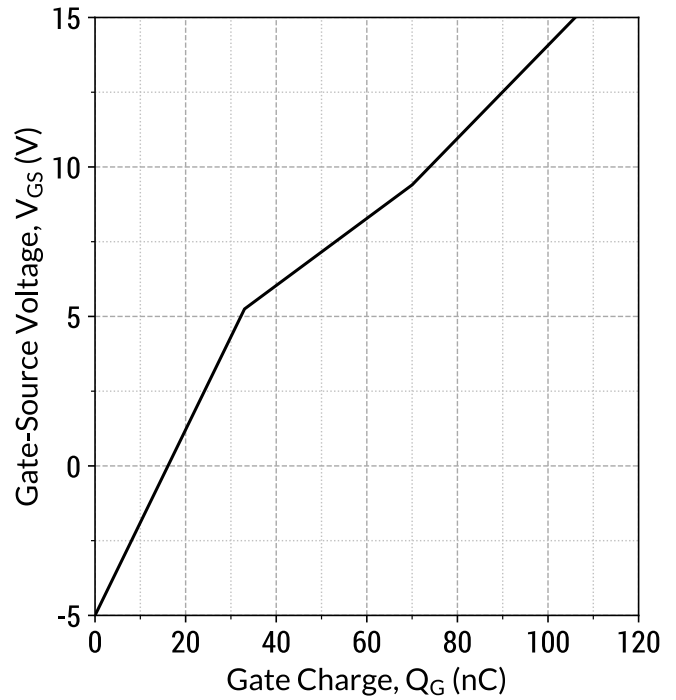


$I_D$ = 35 A; $V_{DS}$ = 1000 V; $T_c$ = 25°C

## Figure 11: Capacitance v/s Drain-Source Voltage
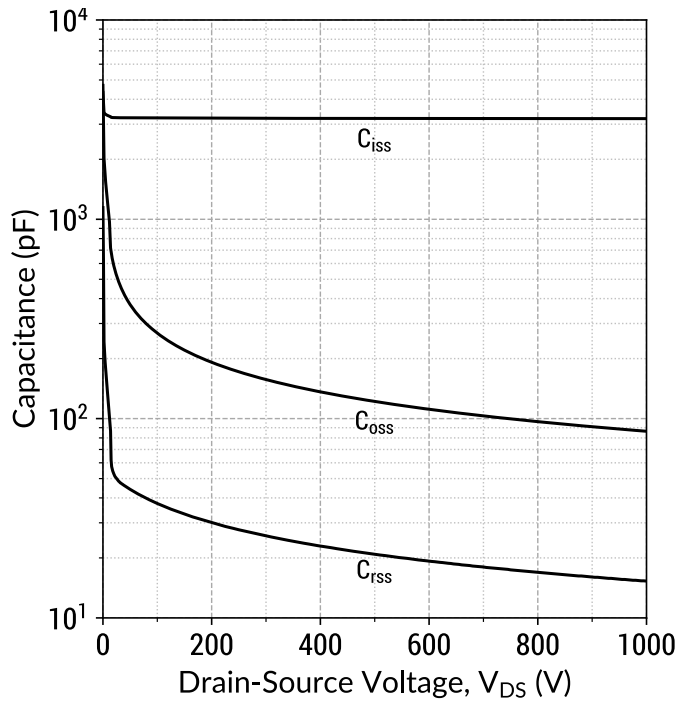


f = 1 MHz; $V_{AC}$ = 25mV

## Figure 12: Output Capacitor Stored Energy
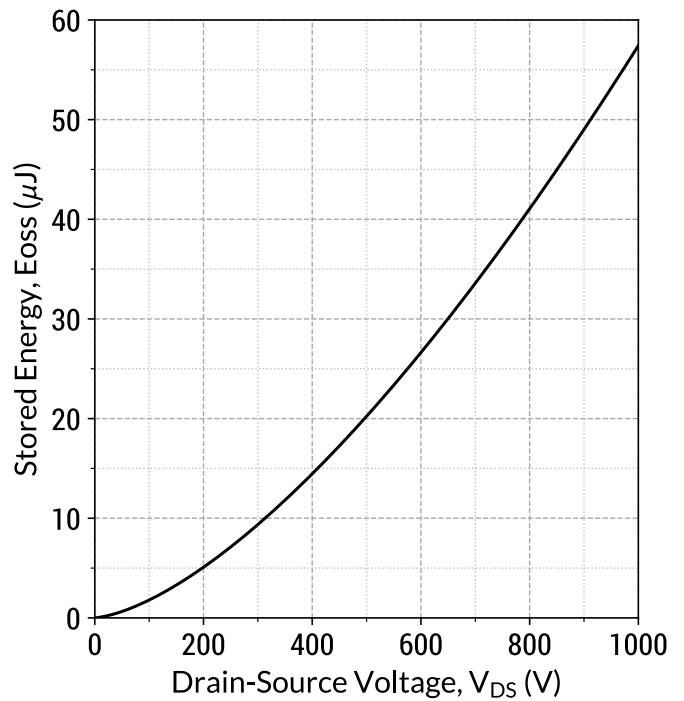


$E_{oss}$ = f($V_{DS}$)
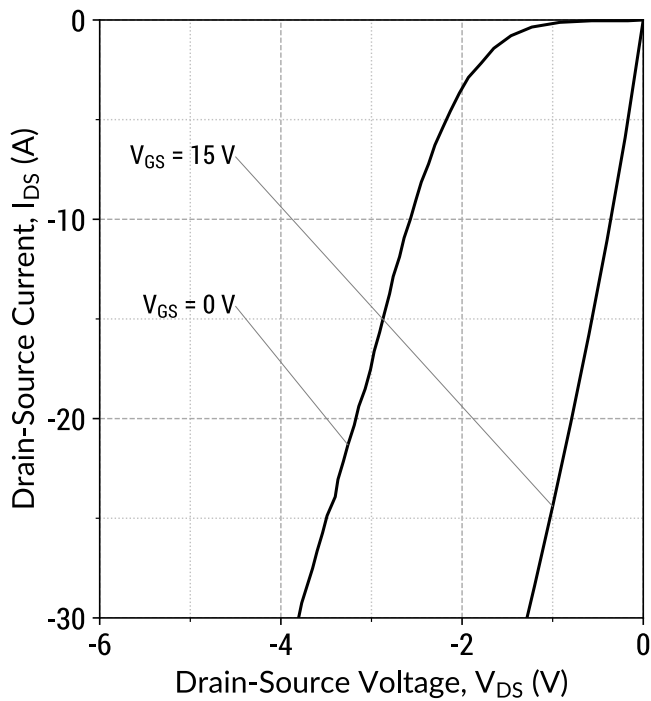
## Figure 13: Body Diode Characteristics (T$_j$ = 25°C)
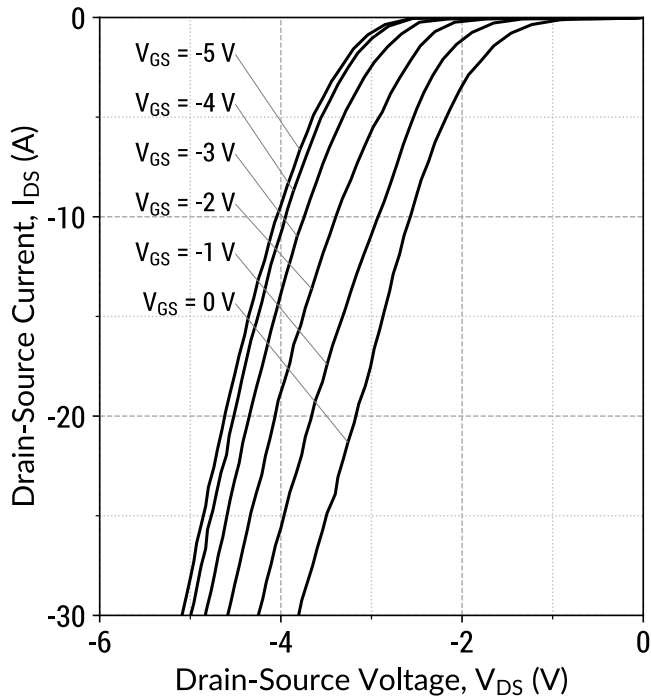


$I_D = f(V_{DS}, V_{GS})$; $t_P = 250$ μs

## Figure 14: Body Diode Characteristics (T$_j$ = 200°C)
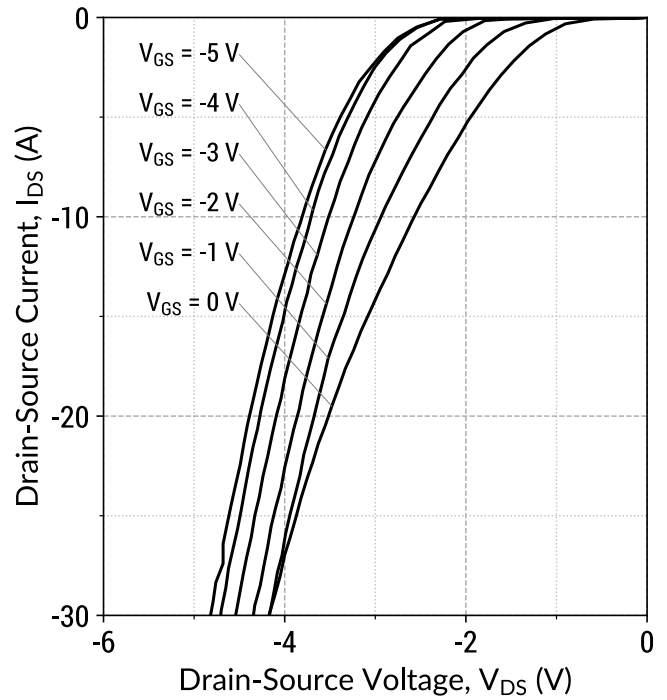


$I_D = f(V_{DS}, V_{GS})$; $t_P = 250$ μs
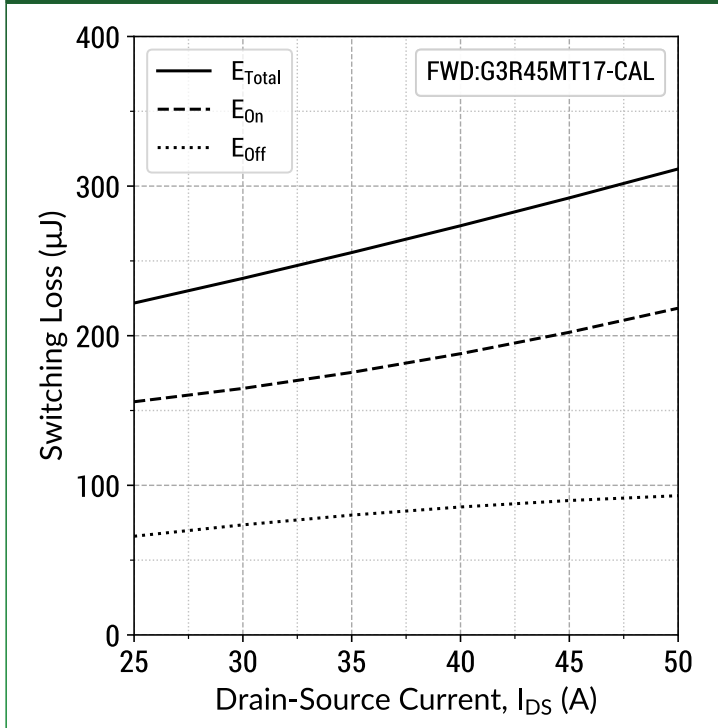
## Figure 15: Third Quadrant Characteristics (T$_j$ = 25°C)



$I_D = f(V_{DS}, V_{GS})$; $t_P = 250$ μs

## Figure 16: Third Quadrant Characteristics (T$_j$ = 200°C)
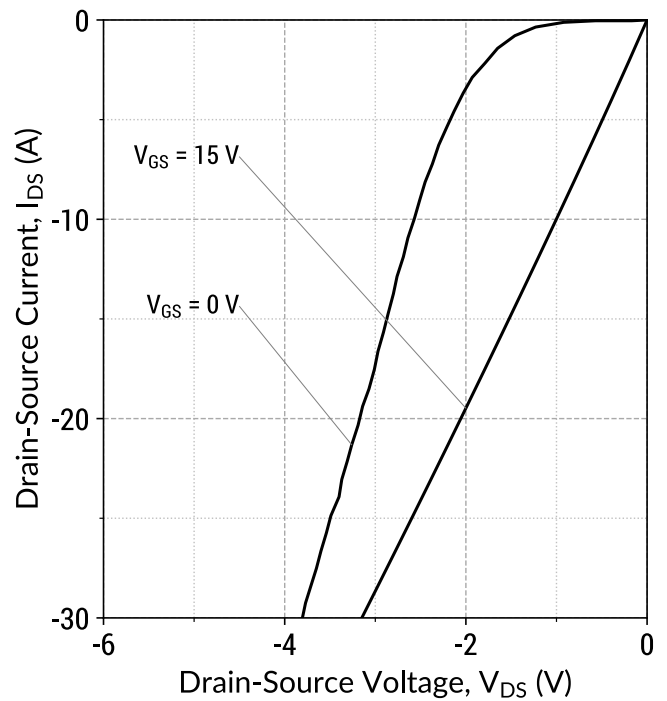


$I_D = f(V_{DS}, V_{GS})$; $t_P = 250$ μs

**Figure 17: Resistive Switching Energy v/s Drain Current ($V_{DD}$ = 1000V)**



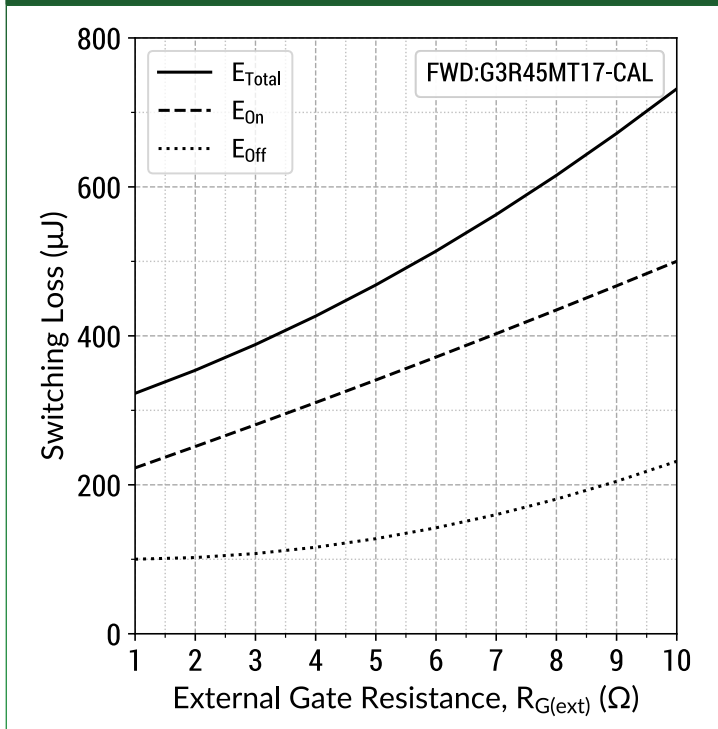$T_j$ = 25°C; $V_{GS}$ = -5/+15V; $R_{G(ext)}$ = 1 Ω

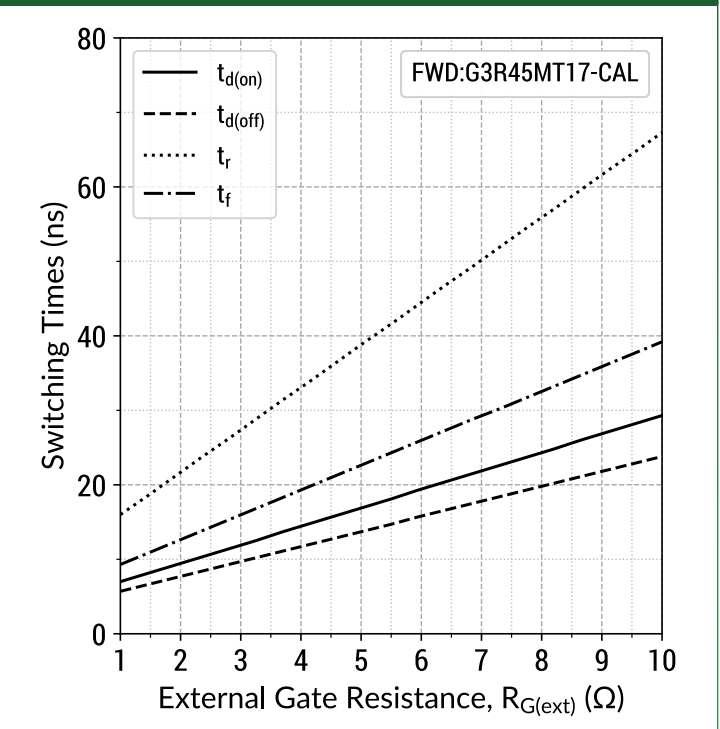**Figure 18: Resistive Switching Energy v/s Drain Current ($V_{DD}$ = 1200V)**
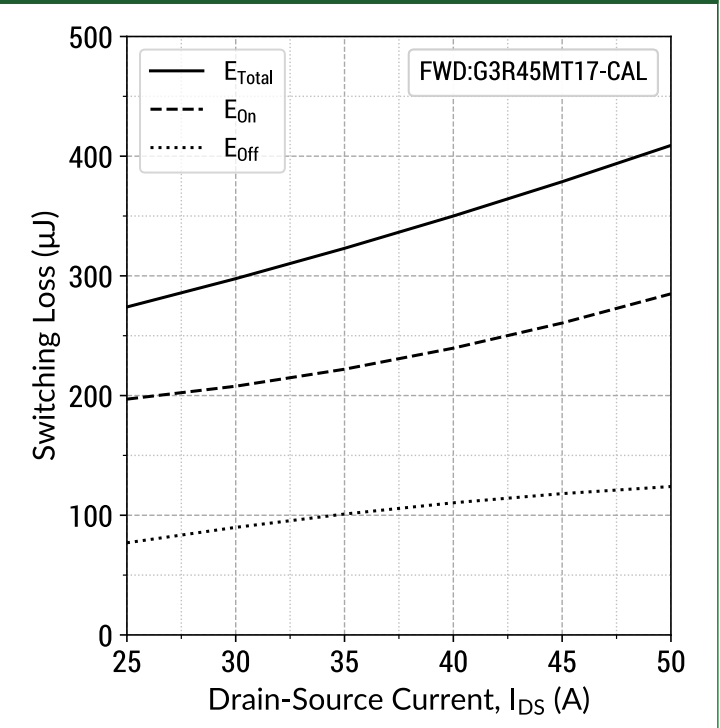


$T_j$ = 25°C; $V_{GS}$ = -5/+15V; $R_{G(ext)}$ = 1 Ω

**Figure 19: Resistive Switching Energy v/s $R_{G(ext)}$ ($V_{DD}$ = 1200V)**

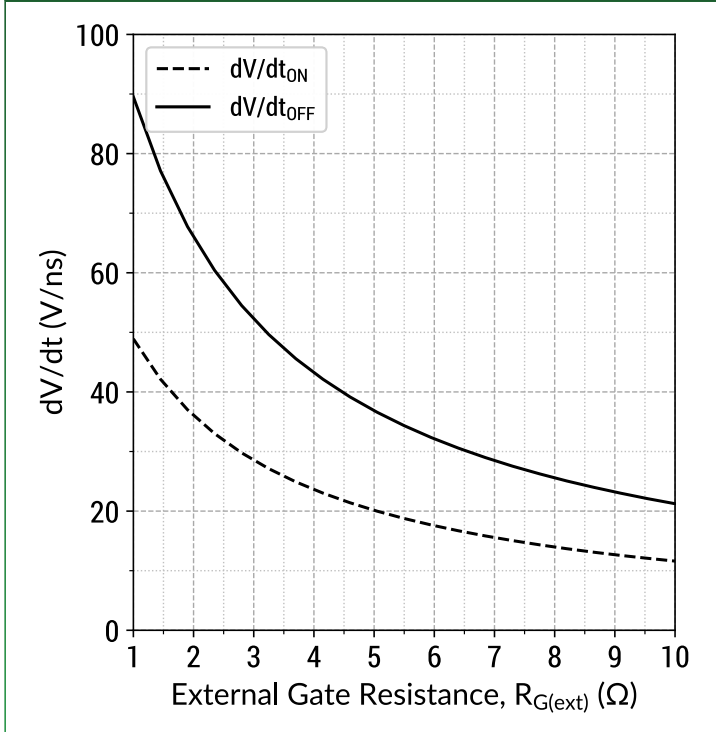

$T_j$ = 25°C; $V_{GS}$ = -5/+15V; $I_{DS}$ = 35 A

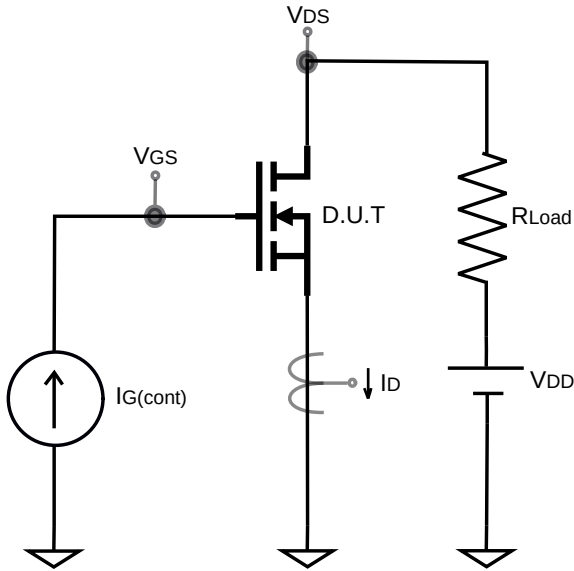**Figure 20: Switching Time v/s $R_{G(ext)}$ ($V_{DD}$ = 1200V)**



$T_j$ = 25°C; $V_{GS}$ = -5/+15V; $I_{DS}$ = 35 A

**Figure 21: dV/dt v/s $R_{G(ext)}$**
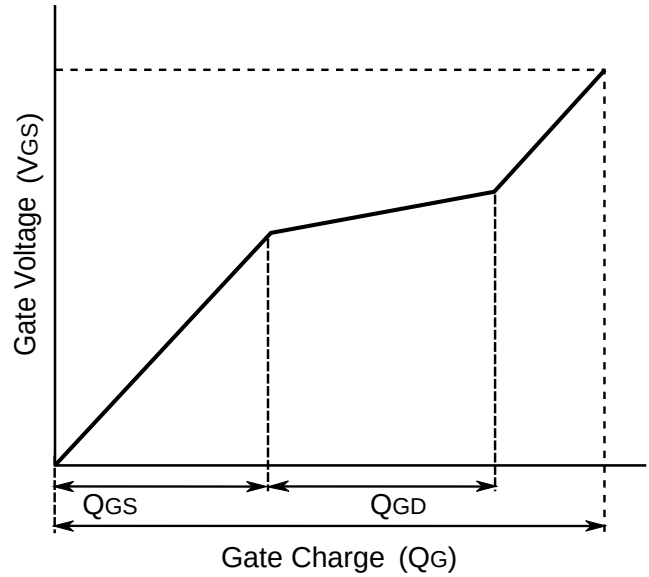**($V_{DD}$ = 1200V)**
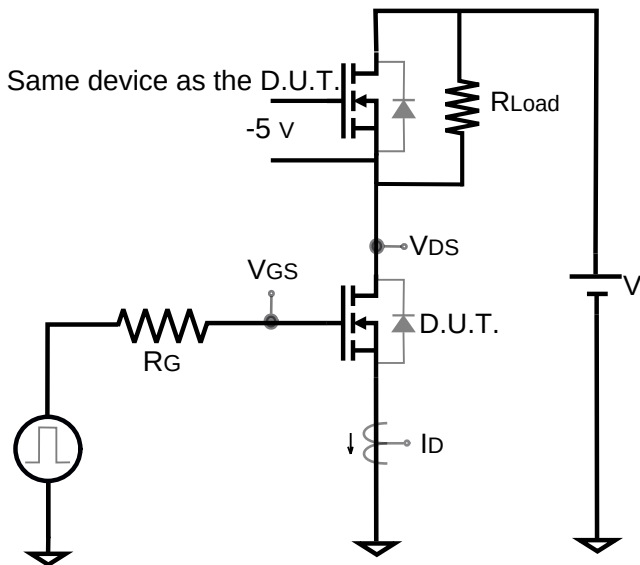


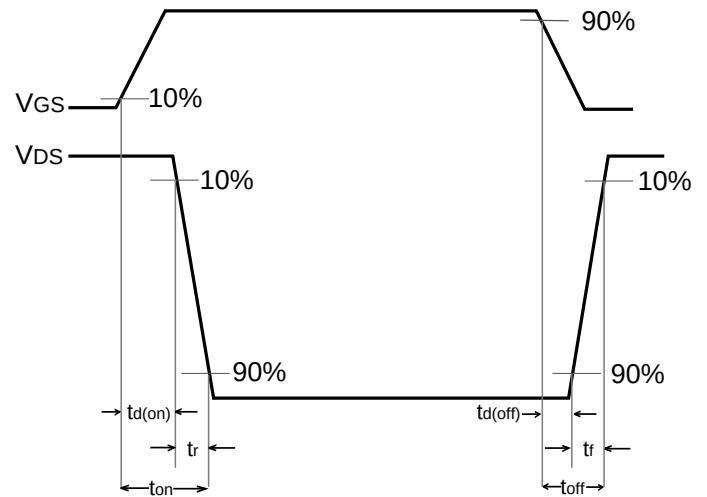$T_j$ = 25°C; $V_{GS}$ = -5/+15V; $I_{DS}$ = 35 A

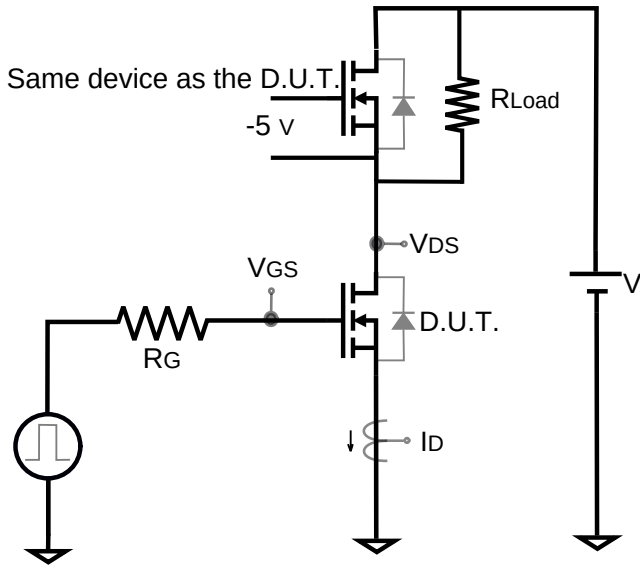## Gate Charge Circuit
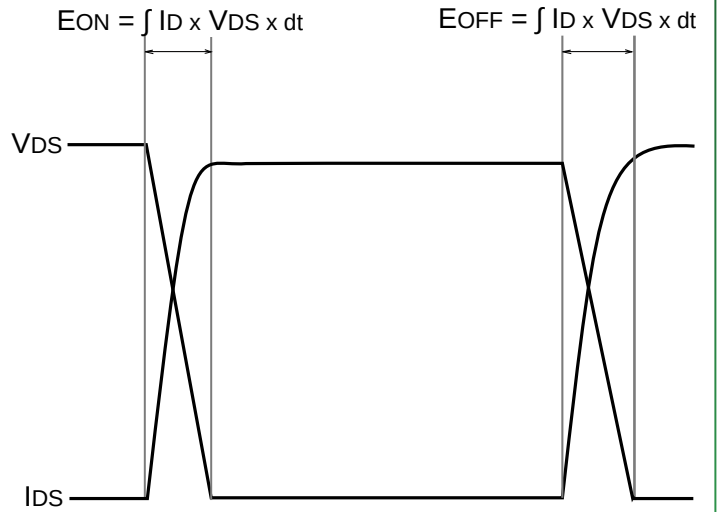


## Gate Charge Waveform



## Switching Time Circuit



## Switching Time Waveform

## Switching Energy Circuit



Same device as the D.U.T.
-5 V
R$_{Load}$
V$_{DS}$
V$_{GS}$
R$_G$
D.U.T.
I$_D$
V

## Switching Energy Waveform



$E_{ON} = \int I_D \times V_{DS} \times dt$

$E_{OFF} = \int I_D \times V_{DS} \times dt$

V$_{DS}$
I$_{DS}$

## Reverse Recovery Circuit



D.U.T.
-5 V
L$_{Load}$
I$_F$
V$_{GS}$
R$_G$
Same device as the D.U.T.
V$_{DD}$
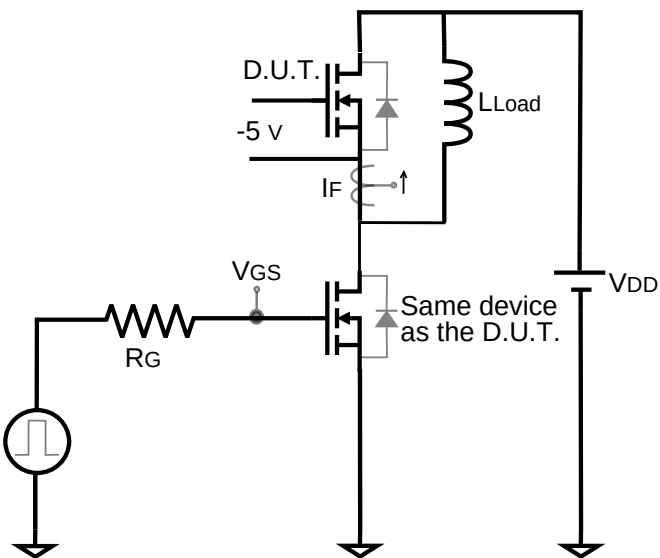
## Reverse Recovery Waveform



I$_F$
0 Level
t$_{rr}$
90%
I$_{rr}$
dI$_{rr}$/dt in 10% to 90% range
10%

# G3R45MT17-CAL
## 1700 V 45 mΩ SiC MOSFET
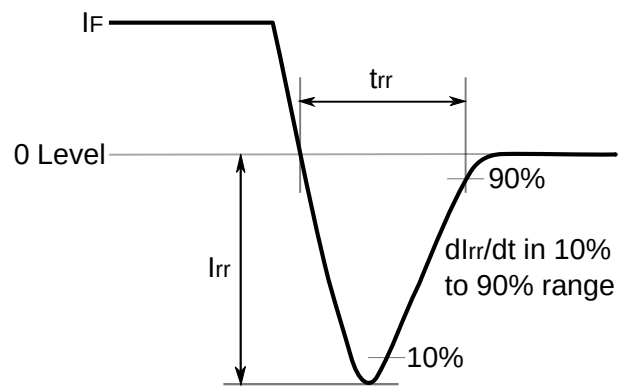
## Mechanical Parameters

This information is confidential, please contact **sales@genesicsemi.com** to learn more.

## Chip Dimensions

This information is confidential, please contact **sales@genesicsemi.com** to learn more.

**NOTE**

1. CONTROLLED DIMENSION IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

## Compliance

### RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

### REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

## Disclaimer

## Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G3R45MT17-CAL/G3R45MT17-CAL_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G3R45MT17-CAL/G3R45MT17-CAL_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-mosfet/G3R45MT17-CAL/G3R45MT17-CAL_3D.zip
- Gate Driver Reference: https://www.genesicsemi.com/technical-support
- Evaluation Boards: https://www.genesicsemi.com/technical-support
- Reliability: https://www.genesicsemi.com/reliability
- Compliance: https://www.genesicsemi.com/compliance
- Quality Manual: https://www.genesicsemi.com/quality

## Revision History

- Rev 21/Jun: Updated switching time and switching energy data
- Supersedes: Rev 20/Jun, Rev 20/Sep, Rev 21/Feb

www.genesicsemi.com/sic-mosfet/

**Rev 21/Jun**
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