S1C17F63

EPSON
EXCEED YOUR VISION

16-bit Single Chip Microcontroller

- Low power operation (110 nA / RTC mode, 450 nA / Sleep mode)
- Built-in EPD driver (voltage booster circuit)
- EPD driving waveform generator
- Real-time clock with theoretical regulation function
- Built-in temperature sensor

■ DESCRIPTIONS

S1C17F63 is a 16-bit embedded Flash MCU that features low power consumption. It includes various types of serial interface, timers, real-time clock and temperature sensor. In addition, it has 42 + 1 segment EPD driver, EPD driving waveform generator.
S1C17F63 is suitable for E-paper applications like Display Card, watch, and tags.

■ FEATURES

Model		
CPU		
CPU core		Seiko Epson original 16-bit RISC CPU core S1C17
Other		On-chip debugger
Embedded Flash Memory		
Capacity		32K bytes (for both instructions and data)
Erase/program count		1,000 times(min.) *Programming by the debugging tool ICDmini
Other		Security function to protect from reading/programming by ICDmini
		On-board programming function using ICDmini
		Flash programming voltage can be generated internally.
Embedded EEPROM		
Capacity		256 bytes
Erase/program count		100,000 times (min.)
Embedded RAM		
Capacity		2K bytes
Clock generator(CLG)		
System clock source		4 sources (IOSC/RTCLP(OSC1)/OSC3/EXOSC)
System clock frequency (operating frequency)		16.8 MHz (max.)
IOSC oscillator circuit (boot clock source)		700kHz(typ.) embedded oscillator
		23 µs(max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
RTCLP clock (OSC1 oscillator circuit)		Clock output from the RTCLP 32.768kHz (typ.) crystal oscillator
		Can be used as the OSC1 clock in the MCU core block
OSC3 oscillator circuit		16, 12, 8, 4, 2, 1, and 0.5 MHz-switchable embedded oscillator
EXOSC clock input		16.8 MHz (max.) square or sine wave input
Other		Configurable system clock division ratio
		Clock external output: 2 channels
		Configurable system clock used at wake up from SLEEP state
		Operating clock frequency for the CPU and all peripheral circuits is selectable
I/O port (PPORT)		
Number of general-purpose I/O ports	I/O port	17 bits (MCU core block) (max.)
	Other	Pins are shared with the peripheral I/O
Number of input interrupt ports		14 bits (MCU core block) (max.)
Number of ports that support universal port multiplexer (UPMUX)		14 bits
		A peripheral circuit I/O function selected via software can be assigned to each port.

Timers		
Watchdog timer(WDT2)		Generates NMI or watchdog timer reset
		Programmable NMI/reset generation cycle
16-bit timer(T16)		4 channels
		Generates the SPIA master clocks and the ADC12A trigger signals
16-bit PWM timer (T16B)		2 channels
		Event counter/capture function
		PWM waveform generation function
		Number of PWM output or capture input ports: 2 ports/channel
Supply voltage detector(SVD3)		
Detection voltage		V_{DD} or external voltage (one external voltage input port is provided and an external voltage level can be detected even if it exceeds V_{DD}.)
Detection level		V_{DD}: 28 levels (1.8 to 5.0 V) / external voltage: 32 levels (1.2 to 5.0 V)
Others		Intermittent operation mode
		Generates an interrupt or reset according to the detection level evaluation
Serial interfaces		
UART (UART3)		1 channels
		Baud-rate generator included
		Open drain output, signal polarity, and baud rate division ratio are configurable
		Infrared communication carrier modulation output function
Synchronous serial interface (SPIA)		2 channels * Ch.0 is also used as the interface with the RTCLP block.
		2 to 16-bit variable data length
		The 16-bit timer(T16) can be used for the baud-rate generator in master mode.
I^2C (I2C)		1 channel
		Baud-rate generator included
Smart card interface (SMCIF)		1 channel
		Baud-rate generator included
Sound generator (SNDA)		
Buzzer output function		512 Hz to 16 kHz output frequencies
		One-shot output function
Melody generation function		Pitch: 128 Hz to 16 kHz ≈ C3 to C6
		Duration: 7 notes/rests (Half note/rest to thirty-second note/rest)
		Tempo: 16 tempos (30 to 480)
		Tie/slur may be specified.
12-bit A/D converter（ADC12A）		
Conversion method		Successive approximation type
Resolution		12 bits
Number of conversion channels		1 channel
Number of analog signal input		7 ports
Number of internal analog signal inputs		1 port (The temperature sensor output is connected.)
Temperature sensor/reference voltage generator (TSRVR)		
Temperature sensor circuit		Sensor output canbe measured using ADC12A
Reference voltage generator		Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, V_{DD}, and external input.
EPD controller/driver (EPDC)		
Number of driver outputs	Segment output	42 outputs
	Top plane output	1 outtput
	Back plane output	1 output
Output voltage		48 levels
Other		Includes a drive power generator.
		Includes a display data memory
		Output drive waveforms can be programmed.
		Supports pin output direct control.
		The segment, top plane, and back plane output pin assignments are selectable.

Independent low-power real-time clock (RTCLP)		
Interface		Register access via SPIA Ch.0.
OSC1 oscillator circuit		32.768 kHz (typ.) crystal oscillator
Oscillation stop detector		Issues a system reset when oscillation stop is detected.
Real-time clock		Second/minute/hour/day/day of the week/month/year counters
		Automatic leap year correction function
		Day/hour/minute/second, alarm, and programmable periodic timer interrupts
I/O ports (P20, P21)		GPIO: 2 bits (max.)
		Input interrupt generation function: 2 bits (max.)
		Pins are shared with the peripheral I/O.
Power management function		MCU power shut down and restart by interruption
Multplier/divider(COPRO2)		
Arithmetic functions		16-bit × 16-bit multiplier
		16-bit × 16-bit + 32-bit multiply and accuulation unit
		32-bit ÷ 32-bit divider
Reset		
#RESET pin		Reset when the reset pin is set to low
Power-on reset		Reset at power on
Brown-out reset		Reset in supply voltage declining
Oscillation stop detection reset		Reset when stop of the OSC1 crystal oscillator is detected.
Key entry reset		Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register)
Watchdog timer reset		Reset when the watchdog timer overflows (can be enabled/disabled using a register)
Supply voltage detector reset		Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register)
Interrupt		
Non-maskable interrupt		4 systems(Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External int.	1 system (8 levels)
	Internal int.	15 systems (8 levels)
Power supply voltage		
V_{DD} operating voltage		1.8 V to 5.5 V
V_{DD} operating voltage for Flash programming		2.2 to 5.5 V (Programming voltage V_{PP}: 7.5 V external voltage or internal boosted voltage)
V_{DD} operating voltage for EEPROM programming		2.2 to 5.5 V (Programming voltage V_{PP}: internal boosted voltage)
Operating temperature		
Operating temperature range		-40°C to 85°C
Current consumption (Typ. Value)		
RTC mode		0.11 µA OSC1 = 32768 Hz, real-time clock = ON, MCU core = OFF
SLEEP mode		0.45 µA IOSC = OFF, OSC1 = 32768 Hz, real-time clock = ON, OSC3 = OFF
HALT mode		0.70 µA IOSC = OFF, OSC1 = 32768 Hz, real-time clock = ON, OSC3 = OFF
RUN mode		5 µA OSC1 = 32768 Hz, real-time clock = ON, CPU = OSC1
		1950 µA OSC3 = 16 MHz, OSC1 = 32768 Hz, real-time clock = ON, CPU = OSC3 (Flash read: 3 cycles)
Shipping form		
1		Gold bump chip (Bump pitch: 85 µm (min.))
2		Aluminum pad chip (Pad pitch: 85 µm (min.))
3		QFP15-100pin (Lead pitch: 0.5 mm)

■ BLOCK DIAGRAM

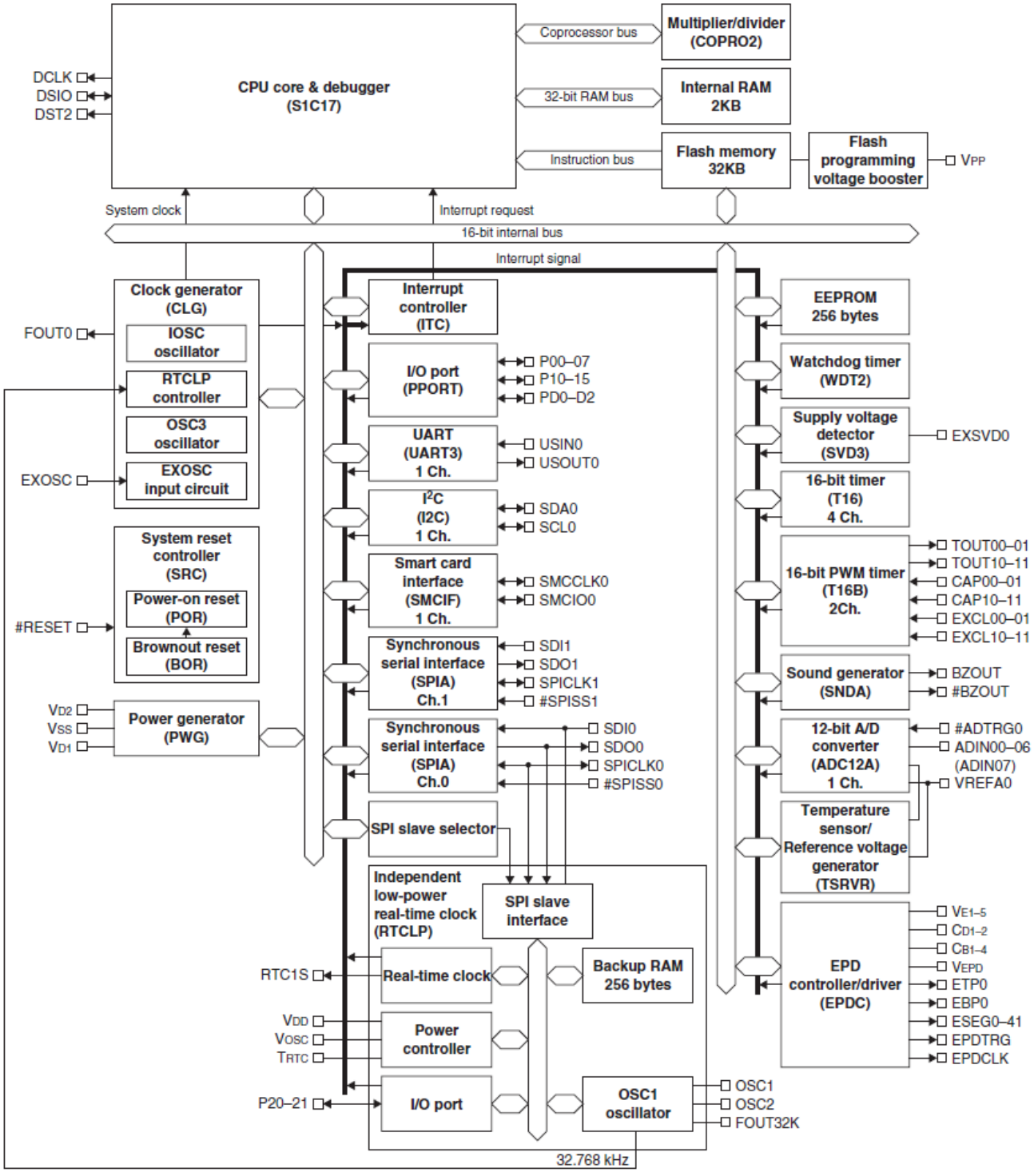


Figure 1 S1C17F63 Block Diagram

■ PIN DESCRIPTIONS

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Tolerant fail-safe structure: = Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter)

Table 1 Pin descriptions

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
V_{DD}	V_{DD}	P	-	-	Power supply (+)
V_{SS}	V_{SS}	P	-	-	GND
V_{PP}	V_{PP}	P	-	-	Power supply for Flash programming
V_{D1}	V_{D1}	A	-	-	V_{D1} regulator output
V_{D2}	V_{D2}	A	-	-	MCU core block operating power supply
V_{D2M}	V_{D2M}	A	-	-	V_{D2} voltage monitor
V_{OSC}	V_{OSC}	P	-	-	V_{OSC} regulator output (OSC1 oscillator power supply)
T_{RTC}	T_{RTC}	A	-	-	V_{OSC} regulator stabilizing capacitor connecting pin
V_{EPD}	V_{EPD}	P	-	-	EPD driver voltage output
V_{E1-5}	V_{E1-5}	P	-	-	EPD power voltage booster outputs
C_{D1-2}	C_{D1-2}	A	-	-	EPD power voltage booster capacitor connecting pins
C_{B1-4}	C_{B1-4}	A	-	-	EPD power voltage booster capacitor connecting pins
OSC1	OSC1	A	-	-	OSC1 oscillator circuit input
OSC2	OSC2	A	-	-	OSC1 oscillator circuit output
#RESET	#RESET	I	I (Pull-up)	-	Reset input
TEST	TEST	I	I	-	Test input
P00	P00	I/O	Hi-Z	-	I/O port
	EPDCLK	O			EPD clock output pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	VREFA0	A			12-bit A/D converter Ch.0 reference voltage input/Reference voltage generator constant voltage output
P01	P01	I/O	Hi-Z	-	I/O port
	EPDTRG	O			EPD trigger output for external EPD driver
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN06	A			12-bit A/D converter Ch.0 analog signal input 6
P02	P02	I/O	Hi-Z	-	I/O port
	BZOUT	O			Sound generator output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN05	A			12-bit A/D converter Ch.0 analog signal input 5
P03	P03	I/O	Hi-Z	-	I/O port
	#BZOUT	O			Sound generator inverted output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN04	A			12-bit A/D converter Ch.0 analog signal input 4
P04	P04	I/O	Hi-Z	-	I/O port
	FOUT0	O			Clock external output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN03	A			12-bit A/D converter Ch.0 analog signal input 3
P05	P05	I/O	Hi-Z	-	I/O port
	SMCCLK0	I/O			Smart card interface clock input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN02	A			12-bit A/D converter Ch.0 analog signal input 2
P06	P06	I/O	Hi-Z	-	I/O port
	SMCIO0	I/O			Smart card interface data input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN01	A			12-bit A/D converter Ch.0 analog signal input 1
P07	P07	I/O	Hi-Z	-	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	VREFA0	A			12-bit A/D converter Ch.0 analog signal input 0

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P10	P10	I/O	Hi-Z	✔	I/O port
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P11	P11	I/O	Hi-Z	✔	I/O port
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P12	P12	I/O	Hi-Z	✔	I/O port
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P13	P13	I/O	Hi-Z	✔	I/O port
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P14	P14	I/O	Hi-Z	-	I/O port
	EXOSC	O			Clock generator external clock input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P15	P15	I/O	Hi-Z	✔	I/O port
	#ADTRG	I			12-bit A/D converter Ch.0 trigger input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	EXSVD0	A			External power supply voltage detection input
P20	P20	I/O	Hi-Z	✔	I/O port
	RTC1S	O			Real-time clock 1-second cycle pulse output
P21	P21	I/O	Hi-Z	✔	I/O port
	FOUT32K	O			Clock external output (32 kHz clock output)
PD0	DST2	O	O (L)	-	On-chip debugger status output
	PD0	I/O			I/O port
PD1	DSIO	I/O	I (Pull-up)	✔	On-chip debugger data input.output
	PD1	I/O			I/O port
PD2	DCLK	O	O (H)	✔	On-chip debugger clock output
	PD2	I/O			I/O port
ETP0	TP	O	Hi-Z	-	EPD top plane output
	BP	O			EPD back plane output
	SEG41	O			EPD segment output
EBP0	BP	O	Hi-Z	-	EPD back plane output
	SEG41	O			EPD segment output
	SEG40	O			EPD segment output
ESEG0	SEG0	O	Hi-Z	-	EPD segment output
	BP	O			EPD back plane output
	TP	O			EPD top plane output
ESEG1	SEG1	O	Hi-Z	-	EPD segment output
	SEG0	O			EPD segment output
	BP	O			EPD back plane output
ESEG2 - ESEG41	SEG2 - SEG41	O	Hi-Z	-	EPD segment output

Note: In the peripheral circuit descriptions, the assigned signal name is used as the pin name.

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

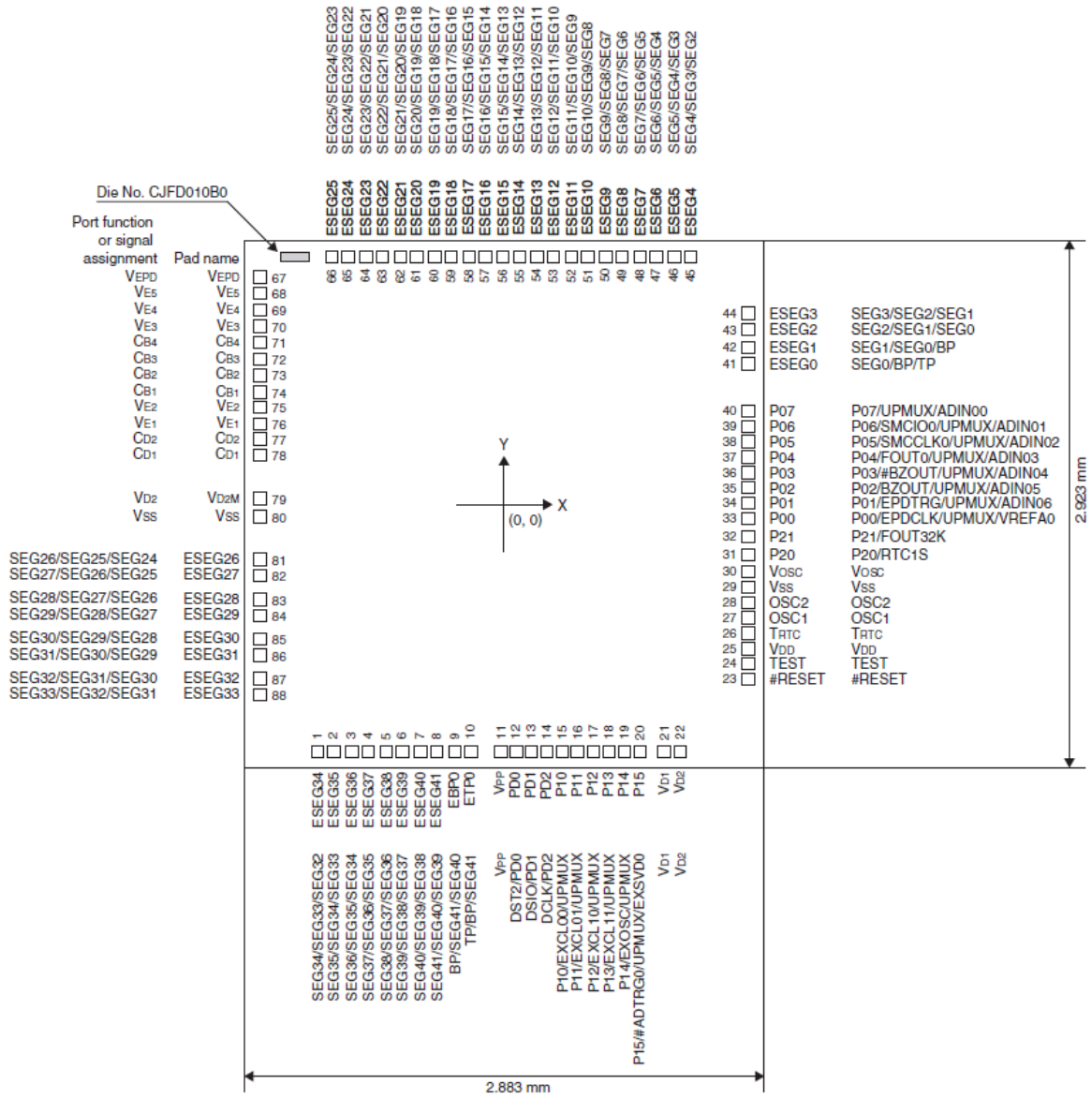
Table 2 Peripheral Circuit Input/output Function Selectable by UPMUX

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
Synchronous serial interface (SPIA)	SDI*n*	I	*n = 0, 1*	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
I^2C (I2C)	SCL*n*	I/O	*n = 0*	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART3)	USIN*n*	I	*n = 0*	UART Ch.*n* data input
	USOUT*n*	O		UART Ch.*n* data output
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n = 0, 1*	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1

Note: Do not assign a function to two or more pins simultaneously.

■ PAD CONFIGURATION DIAGRAM

Aluminum Pad Chip



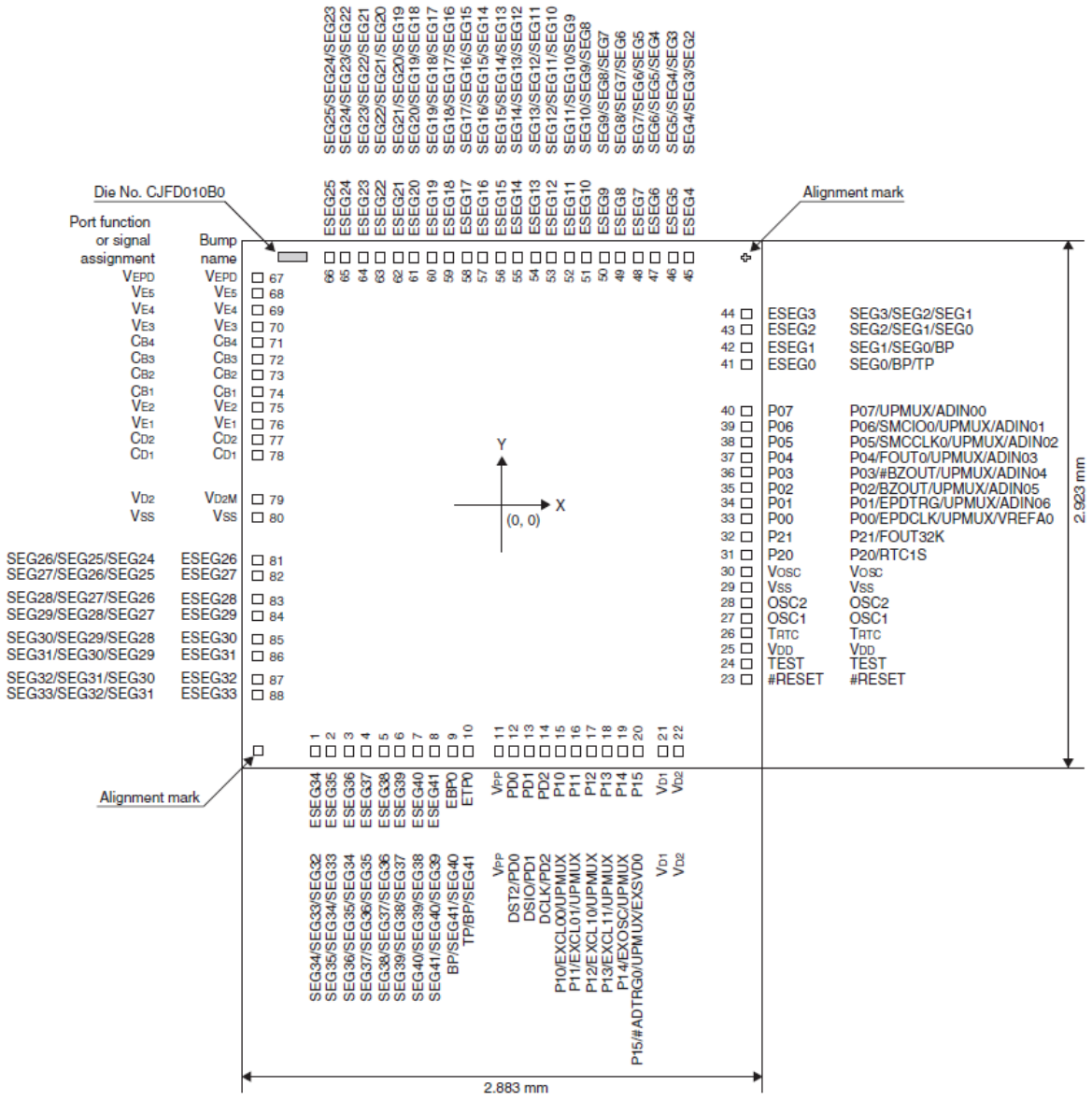
Pad opening X = 68 um, Y = 68 um
Chip thickness 200 um

Figure 2 S1C17F63 PAD Configuration Diagram (Chip)

Table 3 S1C17F63 PAD Coordinates

No.	X um	Y um	No.	X um	Y um	No.	X um	Y um	No.	X um	Y um
1	-1,035	-1,372	23	1,352	-971	45	1,035	1,372	67	-1,352	1,260
2	-945	-1,372	24	1,352	-886	46	945	1,372	68	-1,352	1,170
3	-845	-1,372	25	1,352	-801	47	845	1,372	69	-1,352	1,077
4	-755	-1,372	26	1,352	-716	48	755	1,372	70	-1,352	987
5	-655	-1,372	27	1,352	-631	49	655	1,372	71	-1,352	897
6	-565	-1,372	28	1,352	-546	50	565	1,372	72	-1,352	807
7	-465	-1,372	29	1,352	-461	51	465	1,372	73	-1,352	717
8	-375	-1,372	30	1,352	-376	52	375	1,372	74	-1,352	623
9	-275	-1,372	31	1,352	-281	53	275	1,372	75	-1,352	538
10	-185	-1,372	32	1,352	-181	54	185	1,372	76	-1,352	448
11	-19	-1,372	33	1,352	-81	55	85	1,372	77	-1,352	363
12	66	-1,372	34	1,352	4	56	-5	1,372	78	-1,352	273
13	151	-1,372	35	1,352	89	57	-105	1,372	79	-1,352	33
14	236	-1,372	36	1,352	174	58	-195	1,372	80	-1,352	-67
15	321	-1,372	37	1,352	259	59	-295	1,372	81	-1,352	-305
16	406	-1,372	38	1,352	344	60	-385	1,372	82	-1,352	-395
17	496	-1,372	39	1,352	429	61	-485	1,372	83	-1,352	-525
18	581	-1,372	40	1,352	514	62	-575	1,372	84	-1,352	-615
19	666	-1,372	41	1,352	775	63	-675	1,372	85	-1,352	-745
20	751	-1,372	42	1,352	865	64	-765	1,372	86	-1,352	-835
21	886	-1,372	43	1,352	965	65	-865	1,372	87	-1,352	-965
22	976	-1,372	44	1,352	1,055	66	-955	1,372	88	-1,352	-1,055

Gold Bump Chip



Bump size No. 1-22, 45-66: X = 50 um, Y = 58 um No.23-44, 67-88: X = 58 um, Y = 50 um
Chip thickness 200 um

Figure 3 S1C17F63 PAD Configuration Diagram (Bump)

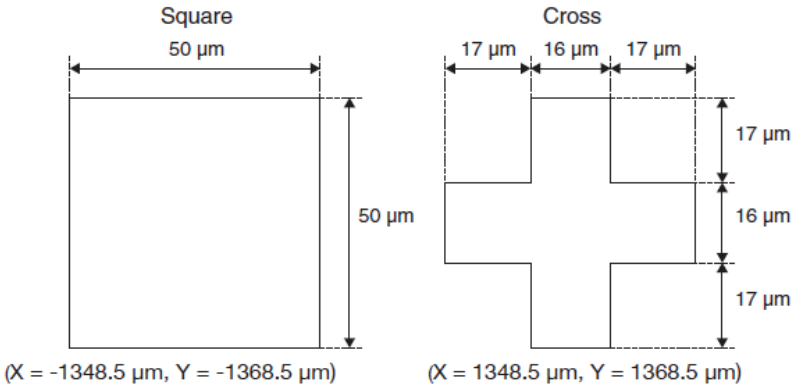


Figure 4 Alignment Mark

Table 4 S1C17F63 Bump Coordinates

No.	X um	Y um	No.	X um	Y um	No.	X um	Y um	No.	X um	Y um
1	-1,035	-1,372	23	1,352	-971	45	1,035	1,372	67	-1,352	1,260
2	-945	-1,372	24	1,352	-886	46	945	1,372	68	-1,352	1,170
3	-845	-1,372	25	1,352	-801	47	845	1,372	69	-1,352	1,077
4	-755	-1,372	26	1,352	-716	48	755	1,372	70	-1,352	987
5	-655	-1,372	27	1,352	-631	49	655	1,372	71	-1,352	897
6	-565	-1,372	28	1,352	-546	50	565	1,372	72	-1,352	807
7	-465	-1,372	29	1,352	-461	51	465	1,372	73	-1,352	717
8	-375	-1,372	30	1,352	-376	52	375	1,372	74	-1,352	623
9	-275	-1,372	31	1,352	-281	53	275	1,372	75	-1,352	538
10	-185	-1,372	32	1,352	-181	54	185	1,372	76	-1,352	448
11	-19	-1,372	33	1,352	-81	55	85	1,372	77	-1,352	363
12	66	-1,372	34	1,352	4	56	-5	1,372	78	-1,352	273
13	151	-1,372	35	1,352	89	57	-105	1,372	79	-1,352	33
14	236	-1,372	36	1,352	174	58	-195	1,372	80	-1,352	-67
15	321	-1,372	37	1,352	259	59	-295	1,372	81	-1,352	-305
16	406	-1,372	38	1,352	344	60	-385	1,372	82	-1,352	-395
17	496	-1,372	39	1,352	429	61	-485	1,372	83	-1,352	-525
18	581	-1,372	40	1,352	514	62	-575	1,372	84	-1,352	-615
19	666	-1,372	41	1,352	775	63	-675	1,372	85	-1,352	-745
20	751	-1,372	42	1,352	865	64	-765	1,372	86	-1,352	-835
21	886	-1,372	43	1,352	965	65	-865	1,372	87	-1,352	-965
22	976	-1,372	44	1,352	1,055	66	-955	1,372	88	-1,352	-1,055

Table 5 Gold Bump Specifications

Characteristic		Specification
Bump shape		Strait bump
Bump height (Distance between Al trace and top of bump)	Central height	15 um Typ.
	Bump-to-bump variation tolerances in all lots	Central height ± 4um
	Bump-to-bump variation tolerances in a chip	R (Max. – Min.) ≦ 3um
Bump hardness	All bumps in all lots	30 to 70 HV
Bump strength	All bumps in all lots	0.0067 g/um^2, shearing within a gold bump
Bump surface asperities	Height Max. – Min. in a bump	3.0 um or less
Bump dimensions	X and Y plane dimension tolerances (at top of bump)	X ± 4 um, Y ± 4 um
Clearance between bumps	Minimum value	S = 20 um

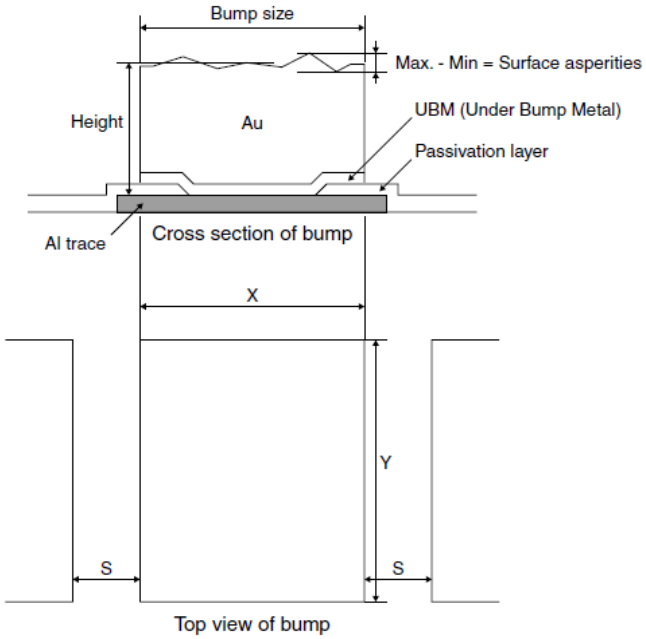


Figure 5 Gold Bump Specifications

■ PIN CONFIGURATION DIAGRAM

QFP15-100pin

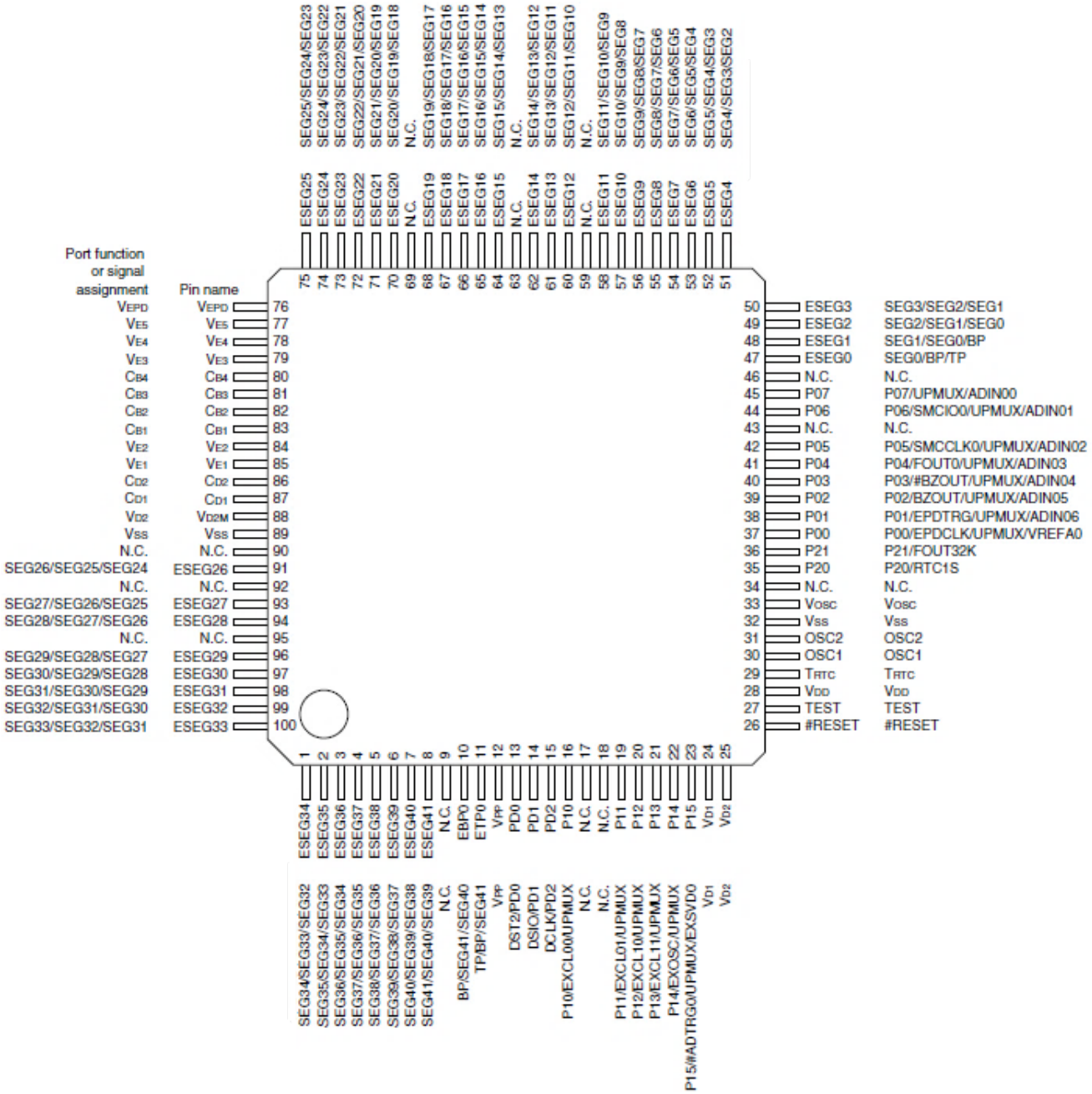


Figure 6 QFP15-100 Pin Configuration Diagram

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